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D E C I S I O N
of 18 November 2002

Case Number: T 0493/00 - 3.4.3

Application Number: 92121508.3

Publication Number: 0602271

IPC: H01L 21/66

Language of the proceedings: EN

Title of invention:
Testing and repairing process for semiconductor memory chips having a redundancy circuit

Applicant:
SAMSUNG ELECTRONICS CO. LTD.

Opponent:
-

Headword:
memory chip/SAMSUNG

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes - after amendments)"
"Skills beyond mere routine to arrive at the claimed process"

Decisions cited:
-

Catchword:
-

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Case Number: T 0493/00 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 18 November 2002

Appellant: SAMSUNG ELECTRONICS CO. LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 14 December 1999 refusing European patent application No. 92 121 508.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: M. Chomentowski
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 92 121 508.3 (publication No. 0 602 271) was refused in a decision of the examining division dated 14 December 1999. The ground for the refusal was that the application did not meet the requirements of inventive step having regard to the prior art documents

D1: New Electronics, Vol. 16, 6 September 1983, pages 19 to 21; and

D3: Siemens Forschungs- und Entwicklungsberichte, Vol. 13, 1984, pages 196 to 200.

II. Claim 1 under consideration in the decision of the examining division reads as follows:

"1. A testing and repairing process for memory chips on a wafer, each chip having redundancy circuits including links and pads for electrical connection,
said process comprising the steps of:
(a) selectively removing, by photography etching process, a passivation film portion disposed over said pads and over said links;
(b) performing a pre-laser test by electrically testing every chip on a wafer through said exposed pads to determine repairable chips on said wafer;
(c) repairing said repairable chips by cutting said links on said repairable chips with a laser beam according to the repairing information obtained by said pre-laser test;
(d) testing a sample of repaired chips after

said laser repairing step to determine a representative goodness ratio per wafer;

(e) quality testing all of said repaired repairable chips to determine which of said repaired repairable chips were unsuccessfully repaired, if said goodness ratio is less than a predetermined value, and omitting said quality testing step if said goodness ratio is greater than or equal to said predetermined value, and

(f) quality marking each of said defective unrepairable chips and each of said unsuccessfully repaired repairable chips determined by said quality testing step."

III. The reasons given in the decision of the Examining Division can be summarized as follows:

(a) Document D1 is considered closest prior art. The method of claim 1 differs from that of document D1 in that (i) each chip is provided with a pad for interconnection and a passivation film is provided over the memory chips which is selectively removed from the pads; (ii) a pre-laser test is performed on every chip and thereafter each repairable chip is repaired; (iii) a sample of the repaired chips are tested, and if the goodness ratio is higher than a certain level, no further testing is carried out, otherwise, all repaired chips are tested; and (iv) marking of all defective unrepairable chips and all unsuccessfully repaired chips.

(b) Differences (i) and (iv) are considered trivial and/or well-known in the art. Difference (ii)

(testing all the chips before repairing is carried out) is only one of a limited number of possibilities, in particular when dedicated equipment for testing and laser repairing, respectively, is used, as in document D1.

(c) As to difference (iii), document D1 states that the chips are retested after repairing. Selecting a sample is suggested in document D3 which is concerned with quality testing and sample testing in particular. If the number of defective items in a sample is greater than a threshold c, then the lot is rejected whereby rejection is followed by one of three options: (a) the entire lot is tested to determine ll defective items ("Sortierprüfung"); (b) the lot is returned to the supplier; or (c) the entire lot is lost. Alternative (a) in document D3 corresponds to steps (d) and (e) of claim 1. There is no sense in retesting chips which have already been determined to be good in the pre-laser test, since this does not produce any new information. Therefore, the skilled person would as a matter of course restrict the quality testing to repaired chips only.

IV. The appellant (applicant) lodged an appeal on 8 February 2000, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 19 April 2000 together with new application documents. The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Claims: 1 to 4 filed with the statement of the grounds of appeal dated 19 April 2000;

Description: pages 1 to 6, 6b, 6c, 7, and 9 filed with the letter dated 7 July 1997, pages 6.1a, 6.2a, and 8 filed with the statement of the grounds of appeal dated 19 April 2000, pages 10 to 14 as filed;

Drawings: Sheets 1/5 to 5/5 as filed.

Furthermore, oral proceedings are requested if the Board is not prepared to grant a patent.

V. Claim 1 according to the appellant's request differs from that under consideration in the decision under appeal in that the feature "each chip having a passivation film, redundancy circuits including links, and pads for electrical connection" in the first paragraph is replaced by (emphasis added by the Board):

"each chip having a passivation film, redundancy circuits including links, and pads for electrical connection **both covered by a passivation film**" .

Claims 2 to 4 are dependent claims.

VI. The appellant essentially presented the following arguments in support of patentability:

(a) Although document D1 describes a testing and repairing process for memory chips, it is silent about integrating this process into a mass-production manufacturing process, in particular about the manufacturing state of the chip to be tested and repaired on a wafer.

(b) Document D3 discloses a sample test which is performed after cutting a wafer into chips and prior to mounting and packaging the chips. This sample test is not provided for determining the quality of an individual chip but only to determine the statistical quality of a lot (i.e. a wafer), and to decide whether a lot has to be accepted or not. In contrast, the present invention teaches not only how to perform a reliable testing and repairing process, but also how the process has to be integrated into the mass production process.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 EPC and Rule 64 EPC and is therefore admissible.

2. *Amendments and Clarity*

Claim 1 is based on claim 1 as filed together with the features disclosed in Figure 6 showing a flow diagram of the claimed process. The Board is satisfied that the requirements of Articles 84 and 123(2) EPC are met.

3. *Inventive step*

3.1 The application in suit relates to a method of repairing memory chips which have so-called redundant cells which can be addressed in place of a faulty memory cell. In a repairing step, the redundant cells are activated by cutting conductive links on the chip with a laser beam. In a process of testing and repairing memory chips acknowledged in the application

in suit, each memory chip is tested twice: A pre-laser test before the repairing step to determine defective but yet repairable chips on a wafer, and a quality test of all the chips after the repairing step (cf. the application in suit, Figure 1; page 4, line 2 to page 5, line 14).

The technical problem addressed by the application in suit relates to reducing the throughput time of a testing and repairing process of memory chips (cf. page 5, line 15 to page 6, line 4, page 6.2a, lines 1 to 11).

The claimed process solves the above problem by modifying the quality testing in such a manner that a sample of repaired chips is first tested to determine a representative goodness ratio per wafer. Further testing of the repaired chips on the wafer is omitted if the goodness ratio is greater than or equal to a predetermined value, and it is assumed that all the repaired chips are good. In case the goodness ratio is less than the predetermined value, all the *repaired* chips on the wafer are tested. In a subsequent step, each of the defective unrepairable chips and each of the unsuccessfully repaired repairable chips are quality marked.

3.2 Document D1 which was considered closest prior art in the decision under appeal discloses a testing and repairing process for memory chips (cf. abstract; page 19). The process of document D1 comprises the steps of:

- performing a pre-laser test wherein a complete memory chip is automatically scanned and checked;

- repairing a defective, repairable chip by cutting links on the chip with a laser beam according to the repairing information obtained by the pre-laser test; and

- testing the repaired chip.

3.2.1 The method according to claim 1 differs from that of document D1 in following features:

(i) a passivation film portion disposed over pads and links is selectively removed by photographic etching process, whereas document D1 does not disclose any passivation film;

(ii) a step of determining repairable chips on a wafer, whereas document D1 does not specify that the individual chips are not already cut from a wafer before being tested;

(iii) after repairing the repairable chips, a sample of repaired chips is tested to determine a representative goodness ratio per wafer, and omitting further testing of the repaired chips on the wafer if the goodness ratio is greater than or equal to a predetermined value, otherwise test all the repaired chips on the wafer, whereas in document D1, each repaired chip is tested; and

(iv) quality marking each of the defective, unrepairable chips and the unsuccessfully repaired chips on the wafer, whereas document D1 is silent as to any marking of defective chips.

3.3 Document D3 teaches the use of sample testing of semiconductor chips, in particular at the stage where the wafer is cut into individual chips and prior to mounting and packaging the chips. As an alternative to testing all the chips of a lot, a sample of *n* chips are tested. When the number of defective items is higher than a predetermined critical number *c*, the lot rejected. One of the possible alternatives how to treat a rejected lot is to test every chip in the lot ("Sortierprüfung") (cf. page 196 "Einleitung").

3.4 In the decision under appeal, it was held that difference (iii) was not considered to be inventive, since document D3 teaches to test the entire lot when the number of defective items in a sample testing is higher than a predetermined critical number *c.* This course of action would correspond to steps (d) and (e) of claim 1 (cf. item III(c) above).

The examining division furthermore reasoned that there would be no sense in retesting chips which have already been determined to be good in the pre-laser step, since this does not produce any new information, and that carrying out the quality testing while the chips are still on the wafer would be considered an obvious alternative.

3.4.1 As convincingly argued by the appellant, however, neither document D1 nor D3 teaches testing the repaired chips on the wafer (cf. items VI(a) and (b) above). Document D1 teaches that the repaired chips are tested after being repaired, but is silent whether the test is carried out before or after the wafer has been cut into individual memory chips. Document D3, on the other hand, describes a testing step carried out after the

wafer has been cut, and where the quality of *all chips* is to be estimated using statistical testing (cf. D3, section 2.1 "Problemstellung").

Therefore, a straightforward combination of the teachings of documents D1 and D3 would result in a quality testing step (e) where a sample is taken from *all* the chips in order to decide whether *all chips* can be approved for the further processing steps or the final test should be carried out on all chips.

3.4.2 As to the argument of the examining division that the skilled person would as a matter of course restrict the quality testing step (e) to repaired chips only, the Board observes that the only available prior art relating to repairing and testing of chips on a wafer is the conventional process as described in the application in suit, where *all* chips on a wafer are quality tested after the repairing step (cf. Figure 1, "Final wafer sorting test"; page 5, lines 9 to 14). Furthermore, the measure of quality testing only the repaired chips requires that the existing process is modified to keep all the results of the pre-laser test step (b), so that all chips can be correctly identified in the subsequent quality marking step (f).

Thus, since neither document D1 nor D3 provides any teaching as to which memory chips on a wafer would be quality tested after the repairing step and the only other available prior art in this respect teaches to test all the chips, the Board comes to the conclusion that the skilled person employing only routine skills would not arrive at the claimed process.

3.5 Therefore, in the Board's judgement, the subject matter

of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents as specified under item IV above.

The Registrar: The Chairman:

P. Martorana M. Chomentowski