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#### DECISION of 11 June 2003

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Case Number:	T 0564/01 - 3.4.
Application Number:	96109828.2
Publication Number:	0750354
IPC:	H01L 29/92

Language of the proceedings: EN

#### Title of invention:

Semiconductor device having capacitor

#### Applicant:

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

#### Opponent:

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#### Headword:

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## **Relevant legal provisions:** EPC Art. 56, 123(2)

# Keyword: "Main request: inventive step (no)" "First and second auxiliary requests: unallowable amendment"

#### Decisions cited:

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#### Catchword:

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Chambres de recours

**Case Number:** T 0564/01 - 3.4.3

#### DECISION of the Technical Board of Appeal 3.4.3 of 11 June 2003

Appellant:	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. 1006, Oaza Kadoma Kadoma-shi Osaka (JP)
Representative:	Kügele, Bernhard Novagraaf SA 25, Avenue du Pailly CH-1220 Les Avanchets - Geneva (CH)
Decision under appeal:	Decision of the Examining Division of the European Patent Office posted 19 December 2000 refusing European application No. 96109828.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman:	R.	К.	Shukla
Members:	V.	L.	P. Frank
	J.	н.	Van Moer

#### Summary of Facts and Submissions

- I. The appeal lies from the decision of the Examining Division dated 19 December 2000 refusing the European patent application No. 96 109 828.2 on the ground that the application did not meet the requirement of inventive step in the sense of Articles 52(1) and 56 EPC. In the decision reference was made *inter alia* to the following prior art documents:
  - D1: Proceedings of the Ultrasonic Symposium, Montreal, Oct. 3-6 1989, vol. 1, 3 October 1989, pp. 299-308
  - D2: Microelectronic Engineering, vol. 19, 1992, pp. 245-252
  - D3: EP-A-0 574 275
- II. The appellant (applicant) lodged an appeal on 5 February 2001, paying the appeal fee the next day. The statement setting out the grounds of appeal was filed on 20 April 2001. Oral proceedings were requested as an auxiliary measure.
- III. During the oral proceedings before the Board the appellant submitted an amended main request consisting of a single device claim, a first auxiliary request consisting of an independent claim to a semiconductor device and an independent claim to a method of fabricating the semiconductor device according to the former claim, and a second auxiliary request consisting of a single device claim.

IV. The independent claims according to these requests have the following wording:

Main request:

"A semiconductor device comprising:

a semiconductor substrate (21) on which an integrated circuit element is formed,

an insulating layer (21a) formed on the semiconductor substrate (21),

a capacitor structure (25) comprising a single continuous bottom electrode (22), a capacitor insulating layer (23) made of one of a ferroelectric material and a dielectric material of high permittivity of layered structure containing Bi, and a single continuous top electrode (24), forming a single capacitor on the insulating layer,

a passivation layer (26) for covering the capacitor (25), having a first hole (27a) formed above the bottom electrode (22) and a second hole (27b) formed above the top electrode (24), and

interconnections (28) connected to the bottom electrode (22) through the first hole and to the top electrode (24) through the second hole respectively,

wherein the end portions of the bottom electrode (22) and the end portions of the capacitor insulating layer (23) are all projecting outside of the end portion of the top electrode (24),

the end portion of the capacitor insulating layer (23) is projecting outside of the end portion of the bottom electrode (22),

the end portion of the capacitor insulating layer(23) is positioned outside of the first hole (27a),

a third hole (29) is formed in a region of the capacitor insulating layer (23) overlapping with the first hole (27a), and

the part of the capacitor insulating layer (23) positioned under the top electrode (24) having a higher crystallinity than the part of said capacitor insulating layer (23) positioned outside of the top electrode (24)."

First auxiliary request:

The independent device claim according to this request differs from the independent device claim of the main request in that the sentence

"the end portion of the capacitor insulating layer projects beyond the end portion of the top electrode for a distance of 0.1 µm or more;"

is inserted after the paragraph of the claim which starts with "wherein the end portions of the bottom electrode ...".

This request further comprises a claim directed to a method of fabricating a semiconductor device according to claim 1.

Second auxiliary request:

The single claim of this request is in substance identical to claim 1 of the first auxiliary request, however, the reference numerals of the insulating layer and the bottom electrode are included in the above mentioned sentence, "the end portion of the capacitor  $\dots 0.1 \ \mu m$  or more".

V. The arguments of the appellant can be summarized as follows:

The application addresses the problem of the deterioration of the capacitor's characteristics due to the degradation of the crystallinity of the capacitor insulating layer. This degradation is due to damage produced at the end portions of the insulating layer by the patterning of the top electrode or by interaction of the end portions with the material of the passivation layer. None of the prior art documents cited addresses this problem.

Moreover, it is well known in the art that the passivation layer adheres poorly to the material used for the capacitor's electrodes. This results in peeling off of the passivation layer. To solve this problem, in the capacitor according to the claims the insulating layer extends beyond the bottom electrode, covering it. The contact area between the electrode and the passivation layer is, therefore, reduced to a minimum.

The appellant's representative argued with respect to the first and second auxiliary requests, that the amendment to the claims is based on the manufacturing method disclosed in the application (cf. column 3, lines 47 to 50) and complies, therefore, with Article 123(2) EPC.

#### Reasons for the Decision

- 1. The appeal is admissible.
- 2. Main request

#### 2.1 Amendments

The amended claim is a combination of claims 1, 3 and 5 as originally filed and the description (cf. column 2, lines 33 to 40 of the published application). It is, however, not expedient to analyse in detail the amendments made to the claim, as the appellant's main request is not allowed for the reasons which follow.

- 2.2 Inventive step (Articles 52(1) and 56 EPC)
- 2.2.1 The application in suit concerns an integrated semiconductor device comprising a capacitor with a ferroelectric or a high permittivity dielectric layer as insulating layer. In a conventional semiconductor device, the crystalline structure of the insulating layer may be damaged during the dry etching step which shapes the capacitor's top electrode or by reaction with the material of the passivation layer. The deterioration in crystallinity of the insulating layer, however, has a detrimental effect on the capacitor's electrical characteristics. To avoid these detrimental effects, the application in suit proposes to extend the insulating layer beyond the top electrode, so that any damaged region is not contained within the capacitor and thereby does not influence its electrical properties (cf. column 1, line 53 to column 2, line 15;

column 2, lines 33 to 40; column 4, lines 18 to 54 and Figure 2 of the published application).

2.2.2 In the decision under appeal, the Examining Division considered that document D3 represents the closest state of the art. The Board concurs with this view and the appellant has not contested it.

> Document D3 discloses a capacitor for a random access memory array in which the capacitor's insulating ferroelectric layer 23 extends beyond the area of the top electrode 24 (cf. D3, column 1, lines 19 to 24; column 6, lines 4 to 54 and Figure 5). Consequently, the end portion of the insulating layer in which the crystallinity might have been deteriorated due to the patterning of the top electrode or due to the interaction with the passivation layer 25 is not contained within the capacitor, and the improvement in the capacitor's electrical characteristics as disclosed in the application in suit is inherently achieved by the capacitor disclosed in document D3. This occurs independently of the reasons for providing the specific arrangement of the layers disclosed in document D3 (ie the reduction in stress due to the thermal expansion of the layers, cf. D3, column 6, lines 34 to 37).

> The technical problem stated in the application in suit (cf. ibid, column 2, lines 11 to 15) is solved, therefore, by the same technical features in document D3 and in the application. Following the established practice of the Boards of Appeal in the consideration of inventive step applying the problem and solution approach, the problem stated in the application in suit, therefore, cannot be regarded as being the

objective technical problem addressed by the claimed invention.

- 2.2.3 The semiconductor device according to claim 1 differs from the device disclosed in document D3 essentially in that:
  - (i) the electric contact to the bottom electrode is made through the insulating layer; and
  - (ii) the insulating layer extends beyond the area of the bottom electrode.

According to the application in suit, by disposing the contact to the bottom electrode within the insulating layer the integration density of the semiconductor device can be increased(cf. column 2, lines 41 to 45).

The application is, however, silent regarding the technical effect achieved by extending the insulating layer beyond the area of the bottom electrode (ie feature (ii)).

2.2.4 The appellant argued that it was well known in the art that the passivation layer, usually a silicon dioxide or silicon nitride layer, has very poor adhesion to the material of the electrodes, usually platinum, and consequently, peeling occurs at the regions in which the passivation layer contacts the electrodes.

> The problem of poor adhesion between a passivation layer and a platinum electrode is mentioned in document D2 even when a titanium adhesion promoter layer is

provided.(cf. D2, page 246, "2. Ferroelectric thin film capacitors", 4th paragraph).

It was further submitted by the applicant that although the feature (ii) is shown in Figure 5 and is not discussed in the description of the application in suit, the skilled person aware of the problem of poor adhesion would clearly derive from the drawing of Figure 5 that by extending the ferroelectric insulating layer beyond the area of the bottom electrode, a direct contact between the electrode and the passivation layer is prevented, and that this in turn reduces peeling of the passivation layer.

The Board finds the above submissions plausible and accepts that the feature (ii) addresses the problem of poor adhesion.

- 2.2.5 The objective technical problem addressed by the application is thus twofold:
  - (i) to increase the integration density; and
  - (ii) to reduce the peeling of the passivating layer.

It follows from the appellant's submissions regarding the problem of poor adhesion that in the embodiment of Figure 4 of document D3, the skilled person would recognize that as the capacitor insulating layer 23 extends to cover only one end portion of the bottom electrode 22 and there is direct contact between the passivation layer 25 and the other end of the electrode, the problem of poor adhesion is only partially solved. It further follows that the skilled person would recognize that the poor adhesion between the passivation layer and the bottom electrode can be further reduced by covering the rest of the bottom electrode by the capacitor insulating layer.

Also, having decided to cover the entire bottom electrode by the capacitor insulating layer, the skilled person has to consider how to provide an electrical contact to the bottom electrode.

Document D1 discloses a ferroelectric capacitor in which the electrical contact to the bottom electrode is made through the ferroelectric insulating layer. This feature makes the capacitor more compact and reduces the area occupied by it (cf. D1, Figure 4b). Thus the provision of an electrical contact to the bottom electrode through the insulating layer was an obvious option available to the person skilled in the art.

- 2.2.6 For the foregoing reasons, in the Board's judgement the subject-matter of the claim according to the main request does not involve an inventive step in the sense of Article 56 EPC.
- 3. First and second auxiliary requests

The independent device claims according to the first and second auxiliary requests are identical in scope. The following discussion will therefore deal with both requests simultaneously.

The capacitor according to claim 1 of these requests comprises an insulating layer which extends beyond the area of the top electrode by at least 0.1  $\mu$ m. It is

further specified in the claim that the bottom electrode and the insulating layer extend both beyond the area of the top electrode, and that the insulating layer extends beyond the area of the bottom electrode.

A capacitor, however, in which the insulating layer extends by at least 0.1 µm beyond the area of the top electrode and simultaneously covers the totality of the bottom electrode is not disclosed in the application in suit. In fact, a capacitor with such a configuration of layers would require specific measures for contacting the bottom electrode, ie a hole in the top electrode aligned with the holes in the passivation and insulating layers to contact the bottom electrode without shorting it with the top electrode. No such measures are, however, disclosed in the application in suit.

For these reasons, it is the Board's judgement that the independent device claim according to the first and second auxiliary requests contains subject-matter which extends beyond the content of the application as filed and therefore contravenes the requirement of Article 123(2) EPC. These requests are, therefore, not allowable.

Order

### For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

U. Bultmann

R. K. Shukla