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D E C I S I O N
of 25 May 2003

Case Number: T 0665/01 - 3.4.3

Application Number: 94830316.9

Publication Number: 0689239

IPC: H01L 21/336

Language of the proceedings: EN

Title of invention:
Manufacturing process for MOS-technology power devices

Applicant:
STMicroelectronics S.r.l., et al

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes - after amendments)

Decisions cited:
-

Catchword:
-

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Case Number: T 0655/01 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 25 May 2003

Appellant: STMicroelectronics S.r.l.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 16 November 2000 refusing European patent application No. 94 830 316.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
J. H. Van Moer

Summary of Facts and Submissions

I. The European patent application No. 94 830 316.9 (Publication No. 0 689 239) was refused by the examining division on 16 November 2000 on the grounds that its subject-matter lacked an inventive step having regard to documents

D1: EP-A-0 481 153; and

D2: US-A-5 217 910,

and, as evidence for general knowledge, documents

D4: S. M. SZE, "Semiconductor Devices Physics and Technology", John Wiley & Sons, 1985, pages 410 and 422; and

D5: S. M. SZE, "VLSI Technology", McGraw-Hill International Editions, 1988, pages 272 to 273.

II. Claim 1 forming the basis of the decision of the examining division reads as follows:

"1. Process for the manufacturing of a MOS-technology power device, characterized by comprising the following steps:

a) forming a conductive insulated gate layer (8) on a surface of a lightly doped semiconductor material layer (3) of a first conductivity type;

b) selectively covering the insulated gate layer (8) with a masking material (20);

c) selectively removing the insulated gate layer (8) from selected portions of the semiconductor material layer (3) surface where the insulated gate layer is not covered by the masking material (20);

d) selectively implanting a first dopant of a second conductivity type into said selected portions of the semiconductor material layer (3), the insulated gate layer (8) and the masking material (20) acting as a mask, in a dose and with an implantation energy suitable to obtain, directly after the implantation and without thermal diffusion steps, heavily doped regions (5) substantially aligned with the edges of the insulated gate layer (8) and the masking material (20);

d) selectively implanting a second dopant of the second conductivity type along directions tilted of prescribed angles (á1, á2) with respect to a direction orthogonal to the semiconductor material layer (3) surface, the insulated gate layer (8) and the masking material (20) acting as a mask, in a dose and with an implantation energy suitable to obtain, directly after the implantation and without thermal diffusion steps, lightly doped channel regions (6) extending under the insulated gate layer (8);

e) selectively implanting a heavy dose of a third dopant of a first conductivity type into the heavily doped regions (5), to form source regions (7) substantially aligned with the edges of the insulated gate layer (8) and substantially internal to the heavily doped regions (5)."

III. The reasoning of the examining division can be summarized as follows:

The application concerns a process of manufacturing MOS-technology power devices. The main object is to solve the problem encountered in prior art processes, i.e. that thermal diffusion of dopants prevents a precise control of their local distribution, rendering a reduction of the local distribution to a submicron range impossible. This object is achieved by implanting dopants with doses and energies and along directions tilted at specific angles with respect to the vertical direction which render it unnecessary to perform any thermal diffusion of the dopants.

The problem that thermal diffusion is disadvantageous for a precise control of the local distribution of dopants in the submicron range in the MOS technology was generally known to people skilled in the art, as can be seen from document D5, which is regarded as an evidence showing that in the art ion implantation is used to replace thermal diffusion.

Document D1 discloses a process for manufacturing a MOS-technology power device comprising the formation of an insulated gate layer (15) by means of masking and etching, the process leading to a device comprising heavily doped regions (14) substantially aligned with the edges of the insulated gate layer (15), channel regions (12) extending under the insulated gate layer (15) and source regions (16) substantially internal to the heavily doped regions (14). The regions (12), (14) and (16) are formed by means of dopant implantation, the insulating gate layer acting as a mask.

The claimed process differs from the process known from document D1 in that:

(I) a masking material used for the definition of the insulated gate layer remains on the top thereof during the steps of forming the heavily doped regions and the channel regions;

(ii) the dopant implantation of the heavily doped regions and the channel regions is performed with doses, energies and, in the case of the channel regions, along directions tilted at prescribed angles, which are suitable to provide these regions without subsequent thermal diffusion steps.

As to feature (I), it is generally known, e.g. from document D4, that photoresist materials can be used as masks for selective ion implantation, so that the skilled person would consider leaving the photoresist mask used for patterning the insulated gate layer during subsequent ion implantations.

Since it was generally known in the art that thermal diffusion is disadvantageous for the manufacture of submicron devices, the skilled person would have consulted document D2 which relates to processes of manufacturing of MOS technology devices which avoid thermal diffusion of dopants. This document teaches the possibility of forming doped regions on a MOS-type device by means of dopant implantation through a mask without following thermal diffusion steps, the heavily doped regions being aligned with the edges of this mask directly after the implantation. It also teaches that lightly doped regions below gate structures of such devices can be formed with precise control of extension and dopant distribution by ion implantation along directions tilted at prescribed angles with respect to

a direction orthogonal to the semiconductor layer surface and without following thermal diffusion steps.

Merely by combining document D1 with the teaching of document D2 and by acting within the framework of his professional skills, the skilled person would arrive at the subject-matter of claim 1 without exercising any inventive skill.

The subject-mater of the dependent claims 2 to 10 was also found to lack an inventive step.

IV. The applicant lodged an appeal against this decision on 11 January 2001, paying the appeal fee on the same day. A statement setting out the grounds of the appeal was filed on 12 March 2001.

V. In response to a communication from the Board issued on 19 March 2003 raising objections under Article 84 and 123(2) EPC against claim 1 of the appellant's requests and proposing amendments to meet these objections, the appellant informed the Board by a telefax received on 22 April 2003 that he agreed to the text of claim 1 as suggested by the Board.

VI. The appellant requested that the decision under appeal be set aside and an patent be granted on the basis of the following application documents:

Description:

Pages 1 to 4, 7, 9, 12 and 13 as originally filed;
Pages 5, 6 and 10 as received on 21 July 1998 with the letter of 17 July 1998;

Pages 8 and 11 as annexed to the communication of the Board dated 19 March 2003 and accepted by the appellant on 22 April 2003;

Claims:

No. 1 as annexed to the communication of the Board dated 19 March 2003 and accepted by the appellant on 22 April 2003;

No. 2 to 10 as received on 21 July 1998 with the letter of 17 July 1998;

Drawings:

Sheets 1/3 to 3/3 as originally filed.

Claim 1 reads as follows:

"1. A process for the manufacturing of a MOS-technology power device, characterized by comprising the following steps:

a) forming a conductive insulated gate layer (8) on a surface of a lightly doped semiconductor material layer (3) of a first conductivity type;

b) selectively removing the insulated gate layer (8) from selected portions of the semiconductor material layer (3) surface;

c) selectively implanting a first dopant of a second conductivity type into said selected portions of the semiconductor material layer (3), the insulated gate layer (8) acting as a mask, in a dose and with an

implantation energy suitable to obtain, directly after the implantation without any thermal diffusion step, heavily doped regions (5) substantially aligned with the edges of the insulated gate layer (8);

d) selectively implanting a second dopant of the second conductivity type along directions tilted of prescribed angles (á1, á2) with respect to a direction orthogonal to the semiconductor material layer (3) surface, the insulated gate layer (8) acting as a mask, in a dose and with an implantation energy suitable to obtain, directly after the implantation and without thermal diffusion steps, lightly doped channel regions (6) extending **only** under the insulated gate layer (8); **said lightly doped channel regions (6) having a dopant concentration that is less than the concentration of said heavily doped regions (5)**;

e) selectively implanting a heavy dose of a third dopant of a first conductivity type into the heavily doped regions (5), to form source regions (7) substantially aligned with the edges of the insulated gate layer (8) **such that direct contact of the source region (7) to the lightly doped semiconductor material layer (3) of the first conductivity type is avoided**."

As compared to claim 1 forming the basis of the decision of the examining division, claim 1 comprises neither information about the masking material (20) selectively covering the insulated gate layer (8) before the steps of selectively removing and implanting, nor about the resulting source regions being substantially internal to the heavily doped regions (5), in the last process step. The features which have been added as compared to the refused

claim 1 have been highlighted by the Board.

Claims 2 to 10 are dependent claims.

VII. The appellant argued substantially as follows in support of his request:

The device fabricated by the process known from document D1 comprises a body region separating the source and drain regions of the opposite conductivity type; the body region extends between the main surfaces of the semiconductor wafer and comprises a lightly doped body portion and a highly doped body portion. In the process of document D1, the lightly doped body portions are formed by implanting dopants using the insulated gate layers as masks. The insulated gate layers and lateral spacers at their sides are used as implantation masks for forming the highly doped body portions. Thermal diffusion of the implanted dopants is necessary for forming the channel regions under the insulated gate layers. As a result of the process the highly doped body portion is inside the low doped body portion, so that the lightly doped channel region formed by the process is not only under the insulated gate electrode.

The structure obtained by the process of document D1 thus comprises a resistance between the base and the emitter of the parasitic transistor formed by the source, the body and the drain of the MOSFET, and this reduces the effectiveness of the short circuit to be made by metallisation contacting the source and body region of the MOS-technology power device.

Using the process of claim 1, wherein the dopants are

directly implanted where they are needed, without any subsequent thermal diffusion, the formation of the resistor arising in document D1 is eliminated.

In the process of document D2, the oblique implantation is not for forming the channel region, which in such a LDD (low doping drain) MOSFET is automatically formed by the semiconductor substrate under the gate, between the source and drain regions, but regions such as portions of the drain regions.

Therefore, the combination of documents D1 and D2 does not lead in an obvious way to the process of claim 1.

Reasons for the Decision

1. The appeal is admissible.

2. *Formal requirements*

Claim 1 of the application as filed specified a "zero thermal budget" process, which expression was explained in the description (see page 12, lines 6 to 14) as meaning that the process is not a "high temperature and long duration" process. Since there is no evidence that the expression is well recognised in the art and since the expression is unclear, it has been deleted for clarity. The claim on the other hand specifies that the implantation steps are effected without any thermal diffusion steps, so that the meaning of the above expression is retained in the claim.

The lightly doped channel regions (6) of the MOS-technology power device manufactured by the process

are now specified as having a dopant concentration that is less than the concentration of the heavily doped regions (5) of the same conductivity type wherein the source regions (7) are formed. It is also now specified that the source regions (7) are substantially aligned with the edges of the insulated gate layer (8) such that direct contact of the source region (7) to the lightly doped semiconductor material layer (3) of the first conductivity type is avoided. These features result in the source region (7) being substantially internal to the heavily doped region (5) and thus not being in contact with the drain region (3) either because the implantation for forming the source regions (7) is not deep enough (cf. Figures 7 and 8) or because photoresist masking parts are put in the corners of the windows in the insulated gate layer (8), as stressed in the description (cf. page 11, lines 4 to 12).

Therefore, in the judgement of the Board, the application satisfies the requirements of Article 123(2) and 84 EPC.

3. *Inventive step*

3.1 The only further issue is that of inventive step.

A process for the manufacturing of a MOS-technology power device is known from document D1 (see Figures 1 to 5 and the corresponding text); the known process comprises in the wording of claim 1 of the request, the following steps, which are designated with the same reference signs as corresponding steps in the claimed process:

(a) forming a conductive insulated gate layer (9) on a

surface of a lightly doped semiconductor material layer (7) of a first conductivity type (n);

(b) selectively removing the insulated gate layer (9) from selected portions of the semiconductor material layer (7) surface;

(d') selectively implanting a dopant of the second conductivity type, the insulated gate layer (9, 15) acting as a mask, in a dose and with an implantation energy suitable to obtain, after the implantation **and after a thermal diffusion step**, lightly doped channel regions (12) extending under the insulated gate layer (9, 15);

(c') selectively implanting a dopant of the second conductivity type into these selected portions of the semiconductor material layer (7), the insulated gate layer (9, 15) acting as a mask, in a dose and with an implantation energy suitable to obtain, after the implantation, heavily doped regions (14) substantially aligned with the edges of the insulated gate layer (9, 15), the lightly doped channel regions (12) having a dopant concentration that is less than the concentration of the heavily doped regions (14);

(e') selectively implanting a heavy dose of a third dopant of a first conductivity type *inter alia* into the heavily doped regions (14), to form source regions (16) substantially aligned with the edges of the insulated gate layer (9, 15) such that direct contact of the source region (16) to the lightly doped semiconductor material layer (7) of the first conductivity type is avoided.

3.2 In the known process, the low-doped channel region (12) under the gate (9, 15) is not formed by oblique implantation without subsequent thermal diffusion, but by selectively implanting a dopant of the second conductivity type (p-) with an implantation orientation which is derivable as not being oblique, and subsequently submitting the semiconductor wafer to thermal diffusion (step d').

This is a main distinguishing feature between the known process and the process of claim 1.

A drawback of the process known from document D1 is that, since it comprises steps of forming spacers (13) at the sides of the insulated gate layer (15) and removal of these spacers (13), it is complicated. Moreover, since the known process comprises steps of thermal diffusion subsequent to the steps of implantation of the dopants, the conditions of the different implantations, the temperatures and durations of the subsequent thermal steps must be taken into account for achieving a MOS-technology power device with the desired characteristics, the process being thus further complicated. Indeed, the examining division had also pointed out with reference to document D5 that the skilled person would be aware that the performance of thermal diffusion was disadvantageous.

In the process of claim 1, these problems are solved by implanting the dopant ions exactly where they are to be put. Thus, the dopants for the channel are implanted directly under the edges of the insulated electrodes, without forming spacers and without thermal treatments subsequent to the implantation steps.

Indeed, it is known from document D2 (see Figures 8A-8F and the corresponding text) to form doped regions (15c, 16c) extending under the edges of the insulated gate layer (14), by selectively implanting a dopant of the corresponding conductivity type along directions tilted of prescribed angles with respect to a direction orthogonal to the semiconductor material layer surface, the insulated gate layer (14) acting as a mask, in a dose and with an implantation energy suitable to obtain, after the implantation and without thermal diffusion steps, lightly doped regions (15c, 16c) extending under the insulated gate layer (14).

However, it is first to be noted that the structure to be fabricated by the process known from document D2 is not a MOS-technology power device with a vertical flow of current between the main surfaces of the wafer, but a conventional MOSFET with the current flowing horizontally along the top surface of the wafer. Document D2 thus concerns a related, but different type of device.

Moreover, the implantation step for implanting dopants under the insulated gate layer is not for forming a channel region, but for forming a region of the same conductivity type as the source or drain region and opposite to the conductivity type of the channel region, in a so called LDD-MOSFET device, i.e., a lightly-doped drain MOSFET. Document D2 thus concerns the fabrication of a related, but different type of region, having a different function.

It is also to be noted that the implantation and subsequent thermal diffusion steps for forming the low doped portion (12) of the body region (14, 12) of the

process of document D1 leads to a highly doped portion of the body region located inside the lightly-doped body portion of the body region. By merely replacing the implantation step and thermal diffusion step of document D1 by an oblique implantation according to document D2, a highly-doped portion located inside the lightly-doped portion is obtained, and this is contrary to the result to be obtained by the process of claim 1 wherein the lightly doped channel region, which corresponds to the lightly-doped portion of the body region, extends only under the insulated gate electrode.

3.3 The following is further to be noted with respect to the structure of the devices discussed in the present decision:

In the device manufactured by the process known from document D1, the (n+, n) drain region (6, 7) of the first conductivity type extends between the bottom surface of the semiconductor wafer, with a drain metallisation (19) formed there, and parts of the opposite, top surface of the wafer located under the insulated gate electrode (9, 15). The (n+) source region (16) is a region of the same first conductivity type formed in this top surface of the wafer and separated from the (n) drain region (6, 7) by a "body" region (12, 14) of the second conductivity type consisting of a highly doped p+ portion (14) formed **inside** a lightly-doped p- portion (12) formed at the same top face of the wafer and, as shown in particular Figures 4 to 7), the highly doped p+ portion (14) of the body region (12, 14) is separated from the drain region by the lightly-doped portion (12) of the body region (12, 14) not only by the part of the low-doped

portion (12) of the "body" region (12, 14) extending under the insulated gate electrode (9, 15), i.e., the effective channel region of the device, but also by the parts of the low doped portion (12) of the "body" region (12, 14), thereby separating in the vertical direction this highly doped portion (14) and the underlying parts of the drain region (6, 7). Indeed, it is disclosed in document D1 (see column 4, lines 3 to 10) that it is an advantage of the process that the junction depth of the high-doping body portion is less than that of the lightly-doped body portion.

It is credible that, as argued by the appellant, the configuration of the low-doped portion of the "body" region underlying the high-doped portion of the body region obtained by the process known from document D1 introduces a resistance between the emitter region and the base region of the parasitic transistor formed by the source region, the body region and the drain region and thus result in ineffective electrical characteristics. This problem is solved in the MOS-technology power device obtained by the process of claim 1, wherein, since the channel region of the second conductivity type is obtained by oblique ion implantation and extends **only** under the gate electrode, the lightly-doped deep body portion has been eliminated. The parasitic transistor is discussed in the application in suit with reference to Figure 1.

However, as set forth here above, the process known from document D2 relates to manufacturing a LDD-MOS (low doping drain) device which is different from the MOS-technology power device known from document D1 and more in particular for forming a portion of the drain thereof, and thus not for forming a channel region. The

process of document D2 is in no way related to the solution of the problem of the deep body region.

A combination of documents D1 and D2 would not therefore be regarded as obvious by a person skilled in the art.

In the decision under appeal, document D4 was relied upon only to show that in semiconductor device technology, photoresist materials are commonly used as masks during ion implantation. The use of photoresist masks during ion implantation with high energies, as claimed in claim 1 of the invention, was therefore regarded as obvious.

Similarly, document D5 was cited in the decision merely to show that in submicron sized devices it was customary and even necessary to replace thermal diffusion of dopants by ion implantation, so that the problem addressed by the claimed invention was not new.

In view of the above, it follows that the above general common knowledge in combination with the process known from document D1 would not lead to the process as claimed in claim 1.

3.4 Consequently, having regard to the state of the art, the subject-matter of claim 1 is not obvious to a skilled person and thus involves an inventive step in the sense of Article 56 EPC.

Therefore, claim 1 is patentable in the sense of Article 52(1) EPC.

Claims 2 to 10 concern particular forms of the process

of claim 1 and are thus also patentable for the same reasons.

Consequently, a patent can be granted on this basis (Article 97(2) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

Description:

Pages 1 to 4, 7, 9, 12 and 13 as filed;
Pages 5, 6 and 10 as received on 21 July 1998 with letter of 17 July 1998;
Pages 8 and 11 annexed to the communication of the Board dated 19 March 2003 and accepted by the appellant on 22 April 2003;

Claims:

No. 1 annexed to the communication of the Board dated 19 March 2003 and accepted by the appellant on 22 April 2003;

No. 2 to 10 as received on 21 July 1998 with letter of 17 July 1998;

Drawings:

Sheets 1/3 to 3/3 as filed.

The Registrar: The Chairman:

N. Maslin R. K. Shukla