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**D E C I S I O N**  
of 16 December 2005

**Case Number:** T 0107/04 - 3.5.02

**Application Number:** 95913556.7

**Publication Number:** 0748537

**IPC:** H03M 3/02

**Language of the proceedings:** EN

**Title of invention:**

Sigma-delta converter having a digital logic gate core

**Applicant:**

Echelon Corporation

**Opponent:**

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**Headword:**

-

**Relevant legal provisions:**

EPC Art. 123(2)

**Keyword:**

"Amendments - added subject-matter (yes)"

**Decisions cited:**

-

**Catchword:**

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Case Number: T 0107/04 - 3.5.02

**D E C I S I O N**  
of the Technical Board of Appeal 3.5.02  
of 16 December 2005

**Appellant:**

Echelon Corporation  
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**Representative:**

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**Decision under appeal:**

Decision of the Examining Division of the  
European Patent Office posted 26 June 2003  
refusing European application No. 95913556.7  
pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** W. Wheeler  
**Members:** M. Ruggiu  
E. Lachacinski

## Summary of Facts and Submissions

I. This is an appeal of the applicant against the decision of the examining division to refuse European patent application No. 95913556.7.

II. The decision under appeal cited in particular the following document of the state of the art:

D1: US-A-4 937 577.

III. In the statement of grounds of appeal, the appellant requested that a patent be granted on the basis of either the main request or the auxiliary request that had been considered in the decision under appeal. In a communication dated 18 July 2005, the board indicated it was unlikely that it would decide to grant the patent in that form. In order to afford the appellant the opportunity to argue his case orally, the board appointed oral proceedings even though the appellant had not requested them. With a letter dated 16 November 2005, the appellant filed a new main request and 1st, 2nd, 3rd, 4th and 5th auxiliary requests. That letter further contained a data sheet dated January 1995 for a dual D-type flip-flop HEF4013B from Philips Semiconductors. During the oral proceedings before the board, which were held on 16 December 2005, after discussion of the main request and the 1st and 2nd auxiliary requests, the appellant withdrew all the requests filed with letter of 16 November 2005 and filed a new set of three claims.

IV. The final requests of the appellant were that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 3 filed during the oral proceedings before the board (main request), or on the basis of a single claim consisting of the combination of claims 1 to 3 filed during the oral proceedings (auxiliary request).

V. Claims 1 to 3 filed at the oral proceedings of 16 December 2005 read as follows:

1. "A  $\Sigma$ - $\Delta$  oversampled A/D converter circuit comprising the following four elements ( a) - d)) arranged consecutively and functionally separated from each other in the conventional manner:

a) an integrator (304; 702; 806; 901, 902) for integrating an analog input signal (x(t)) to produce an integrated signal, said integrator comprising an unbuffered inverter implemented by a single digital logic gate (602; 801);

b) a one-bit quantizer (305; 704) for quantizing said integrated signal to produce a quantized signal, the input of said quantizer being coupled to the output of said integrator (304; 702; 806; 901, 902);

c) a sampler (306; 705; 812) for sampling said quantized signal to produce a sampled signal, said sampler being a conventional D-Flip-Flop having - as usual - an inverter at its input the input of said sampler being coupled to the output of said quantizer (305; 704); and

d) a decimator (302) for decimating said sampled signal and for outputting a digital signal  $x(n)$  representative of an amplitude of said analog signal  $x(t)$ , the input of said decimator being coupled to the output of said sampler (306; 705; 812);

characterised in that

e) said quantizer (305; 704) is a buffer implemented by a single digital logic gate (501; 811); and

f) said quantizing logic gate buffer (501; 811) as well as said logic gate inverter (602; 811) of said integrator are standard logic gates of the same common gate array."

2. "The converter circuit of claim 1, characterised in that said integrator (901, 902) is contained in a loop filter circuit having an open loop transfer function with a peak corresponding to a frequency wherein noise in the converted signal is minimized."

3. "The converter circuit of claim 2, characterised in that said transfer function has a pair of complex poles."

VI. The arguments of the appellant that are relevant to the amendments made in order to arrive at the claims according to the present requests can be summarised as follows:

The original application documents, especially Figures 3, 5 and 7 to 9 in connection with their description, supported the amendments made to the

claims. Starting at line 8 of the paragraph bridging pages 16 and 17, the originally filed description disclosed that the sampler was a flip-flop. Both Figure 8 and Figure 9 of the application as filed showed that the sampler flip-flop was a D-flip-flop. As a rule, the first element within a D-flip-flop, i.e. the first element after its input terminal, was always an inverter gate (or inverting buffer), which was usually followed by further inverter gates within the D-flip-flop. This was evidenced by e.g. Figure 6A of document D1 and the explanations in column 7, lines 54 to 58 of D1, and by the data sheet of the dual D-type flip-flop HEF4013B filed with letter of 16 November 2005. Thus, the amendments did not contravene Article 123(2) EPC.

### **Reasons for the Decision**

1. The appeal is admissible.
  
2. The application as filed mentions a flip-flop in a passage starting at line 8 of the paragraph bridging pages 16 and 17. This passage reads as far as the end of the paragraph as follows (underlining by the board):  
"The output from buffer 811 is coupled to a flip-flop 812. Flip-flop 812 comprises the sampler. In the currently preferred embodiment, a sampling rate  $F_s$  of 10 MHz is used. The signal from flip-flop 812 is driven by buffer 813 and output to the digital filter/decimator. Lastly, resistor 814 functions as 1 bit D/A converter converting the sigma-delta output back to analog form for summing with the input at summing node 800. The feedback loop is negative due to

the unbuffered inverter 801 of integrator 806. Note that the unbuffered inverter 801, CMOS buffer/comparator 811, flip-flop/sampler 812, and driver 813 components can all be fabricated out of standard digital gate array logic cells. Furthermore, these gate array cells can be part of a larger device (e.g., a modem, transceiver, instrument, processor, etc.)."

The term "flip-flop" does not appear at any other place in the description and claims of the application as originally filed. In Figure 8 of the originally filed application, a "D" is placed near the input of the element carrying reference numeral 812. A corresponding element in Figure 9, which does not carry a reference numeral, also includes a "D" near its input.

3. A flip-flop, and a D-flip-flop in particular, is essentially a circuit that has two stable states, with means for passing from one state to the other under control of external signals. It can be true that some or even most D-flip-flops have an inverter as first element at the input, as shown in document D1 and in the data sheet provided with the letter of 16 November 2005. However, in the view of the board, the skilled person would regard the term "flip-flop", as used in the context of the application as filed, essentially as an indication of a particular function, independently of the specific circuit used to implement this function. Thus, the skilled person would not consider it essential or implicit that the flip-flop must include its own internal inverter at its input. The application as filed does not mention that an inverter is present as the first internal element at the input of the flip-

flops shown in Figures 8 and 9 and does not provide any hint that this could be of importance for the invention. The application as filed also does not indicate whether the flip-flops shown in Figures 8 and 9 are implemented by conventional circuits or not. Thus, in the judgment of the board, the application as filed does not disclose that the D-flip-flop 812 shown in Figure 8 or the D-flip-flop shown in Figure 9 is a conventional D-flip-flop including an inverter at its input. Therefore, claim 1 of the main request and the single claim of the auxiliary request contain subject-matter extending beyond the content of the application as filed and thereby contravene Article 123(2) EPC.

**Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:

U. Bultmann

W. J. L. Wheeler