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# Datasheet for the decision of 4 September 2008

**Case Number:** T 0858/04 - 3.5.04

**Application Number:** 95113168.9

**Publication Number:** 0700042

**IPC:** G11B 20/10

**Language of the proceedings:** EN

**Title of invention:**
Signal processing device

**Applicant:**
CANON KABUSHIKI KAISHA

**Opponent:**
-

**Headword:**
-

**Relevant legal provisions:**
RPBA Art. 13

**Relevant legal provisions (EPC 1973):**
EPC Art. 56

**Keyword:**
"Inventive step (no)"
"Late filed request - admitted (yes)"

**Decisions cited:**
-

**Catchword:**
-

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**Case Number:** T 0858/04 - 3.5.04

# D E C I S I O N
**of the Technical Board of Appeal 3.5.04**
**of 4 September 2008**

**Appellant:** CANON KABUSHIKI KAISHA
30-2, 3-chome, Shimomaruko
Ohta-ku
Tokyo (JP)

**Representative:** TBK-Patent
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 11 February 2004 refusing European application No. 95113168.9 pursuant to Article 97(1) EPC 1973.**

**Composition of the Board:**

**Chairman:** F. Edlinger
**Members:** M. Paci
B. Müller

## Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse European patent application No. 95 113 168.9.

II. The decision under appeal was based on the ground that the subject-matter of claims 1 and 13 did not involve an inventive step (Article 56 EPC 1973) in view of the state of the art disclosed in

D2: US-5 265 125 A.

III. With the statement of grounds of appeal the appellant filed a set of amended claims replacing the claims on which the appealed decision had been based.

IV. In an official communication accompanying the summons to oral proceedings the board expressed doubts that the amended claims complied with Article 84 EPC 1973 and Article 123(2) EPC.

V. With a letter dated 28 July 2008 the appellant filed amended claims 1 and 13 and reverted to dependent claims 2 to 12 and 14 to 24 as originally filed.

VI. Oral proceedings were held before the board on 4 September 2008.

VII. Independent claim 1 reads as follows:

"A digital signal processing device comprising:
a magnetic head (2) adapted to reproduce a digital signal from a magnetic tape (1);

a gain control amplifier (3) adapted to control the amplitude of the reproduced digital signal;

a reproduction equalizing circuit (4) adapted to integrally equalize the amplitude controlled reproduced digital signal;

an A/D converter (5) adapted to sample the integrally equalized amplitude controlled reproduced digital signal;

**characterized by** a digital amplitude detecting circuit (40) comprising

a) pattern detecting means (412; 515; 517) adapted to detect a specific pattern included in said sampled integrally equalized amplitude controlled reproduced digital signal;

b) level detecting means (413; 516) adapted to detect the level of the digital signal on the basis of an output of said pattern detecting means; and

c) level control means (423; 525) adapted to control said gain control amplifier (3) according to an output of said level detecting means."

VIII. The appellant's final request is that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

- claims 1 and 13 as filed with the letter dated 28 July 2008;
- claims 2 to 12 and 14 to 24 as originally filed;
- description pages 7 and 8 as filed on 19 December 2003;
- description pages 1 to 6 and 9 to 23 as originally filed; and
- drawing sheets 1/10 to 10/10 as originally filed.

IX. The examining division's reasoning in the appealed decision, as far as it is still relevant to present amended claim 1, can be summarised as follows.

Starting from the embodiment shown in figure 9 of D2 it would be obvious to control the amplification level of the pre-amplifier (2) instead of the reference levels in the Viterbi decoder (58). The other distinguishing feature of claim 1, according to which the A/D converter output is converted to a higher-level partial response signal from which the zero level is removed via pattern detection, has no effect on the determined amplitude level A. The applicant has not shown, or even shown to be plausible, why the gain control signal in the embodiment shown in figure 4 of the present application should be different from that of low pass filter 57 in figure 9 of D2, even though more hardware is used. Since this additional hardware has no effect on the control signal, no inventive step can be discerned in this characterising feature of claim 1.

X. The appellant argued essentially as follows.

D2 suggests neither the pattern detecting means nor the gain control amplifier of claim 1. The device of D2 solves the problem of keeping the amplitude of the reproduced signal constant by detecting the amplitude "at the data detecting moment", instead of detecting the amplitude of the envelope of the signal. Hence no indication whatsoever is given to further develop the amplifier 2 towards the gain control amplifier used in a closed loop as in the present invention.

## Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of late-filed amendments*

Present amended claims 1 and 13 were filed by the appellant with the letter dated 28 July 2008, approximately six weeks before the date of the oral proceedings. The board considered that the amendments overcame objections of added subject-matter and lack of clarity raised in the official communication accompanying the summons to oral proceedings and that they added no complexity to the case. Accordingly the board exercised its discretion under Article 13(1) and (3) RPBA (see OJ EPO 2007, 536) in admitting the late-filed amendments.

3. *Construction of claim 1*

The "pattern detecting means" in feature a) of claim 1 are adapted to detect a specific pattern in the digital signal output by the A/D converter (see, for example, figure 4). The claim does not define the "specific pattern". The only contextual information derived from other features of claim 1 is that the gain control amplifier is adapted to control the amplitude of the reproduced digital signal in which this specific pattern has been detected, which is no concrete limitation of the form the pattern may take. The "pattern detecting means" thus have a broad meaning which might be objectionable at least under Article 84 EPC. However this matter need not be decided upon by the board because, based on a technically sensible

interpretation of the expressions "pattern detecting means" and "specific pattern", the board came to the conclusion that embodiments covered by claim 1 did not involve an inventive step (see reasoning below).

4. *Inventive step (Article 56 EPC 1973)*

4.1 D2 discloses, in the embodiment shown in figure 9, a digital signal processing device having a magnetic head (1) for reproducing a digital signal from a recording medium (see column 3, lines 24 to 26), an amplifier (2) receiving the output of the magnetic head, a reproduction equalising circuit (20) connected to the output of the amplifier and adapted to integrally equalise the reproduced digital signal (see D2, figure 2(a) to 2(c) and column 3, lines 28 to 51; see also figure 2 and column 1, lines 31 to 49 of the published application), an A/D converter (22) for sampling the output of the equalising circuit in synchronism with a clock signal (103) synchronised with the digital information bit (see column 5, lines 6 to 12 and 51 to 53), a digital partial response equaliser (53) and a Viterbi decoder (58). Moreover fluctuations in the amplitude of the reproduced signal are compensated for by an amplitude detector (55) comprising an absolute value circuit (56) for obtaining the absolute value of the sampled signal (131) output by the A/D converter and a low pass filter (57) for smoothing the output of the absolute value circuit and delivering an amplitude information signal (133) to the Viterbi decoder. Reference levels inside the Viterbi decoder are then adjusted on the basis of the amplitude information signal, thereby compensating for

fluctuations in the amplitude of the reproduced signal (see column 5, lines 58 to 68).

4.2 It is undisputed that the above digital signal processing device of D2 represents the closest prior art with respect to claim 1.

4.3 The digital signal processing device of claim 1 thus differs from the above device of D2 by the following features:
(i) the recording medium is a magnetic tape;
(ii) the amplifier is gain controlled and
(iii) there are pattern detecting means adapted to detect a specific pattern in the digital signal output by the A/D converter, level detecting means adapted to detect the level of the digital signal on the basis of an output of the pattern detecting means and level control means adapted to control the gain control amplifier according to an output of said level detecting means.

4.4 Feature (i) represents an obvious use of the magnetic head (1) in D2 because magnetic tapes were among the most commonly used magnetic recording media at the priority date of the present application.

4.5 According to the description of the present application (see page 7, last paragraph to page 8, paragraph 3), features (ii) and (iii) attempt to solve the problem of undesired fluctuations in the amplitude level of the reproduced signal.

The device shown in figure 9 of D2 also addresses a problem of fluctuations in the amplitude of the

reproduced signal (see from column 1, line 43, to column 2, line 2 of D2). However it solves the problem in a different way in that the detected amplitude is used for adjusting the reference levels inside the Viterbi decoder (see point 4.1 above).

The solution adopted in claim 1 differs from that of D2 in that the level of the digital signal output is detected on the basis of an output of the pattern detecting means and is used for adjusting the gain of the amplifier at the output of the magnetic head, thus forming a closed loop automatic gain control (AGC; referred to as GCA in figure 4) which keeps the amplitude of the reproduced signal constant.

At the priority date of the application closed-loop AGCs were undisputedly a well-known technique for keeping the amplitude of a signal constant (see, for instance, the prior art shown in figure 1 of the present application). The skilled person would therefore have regarded the use of the amplitude information signal (133) to control the gain of amplifier 2 as an obvious alternative to controlling the reference levels in the Viterbi decoder in the device of figure 9 of D2.

D2 does not disclose the internal structure of the absolute value circuit (56) shown in figure 9. The sampled reproduced signal (131) should normally have a value of either +A or -A, depending on its binary value, because sampling is carried out at a time free from inter-symbol interference (see D2, column 4, lines 1 to 13, and column 5, lines 61 to 64). The amplitude measured by the absolute value circuit (56) should thus

normally be equal to A. However, as was well known to the skilled person, noise would also be present in the sampled signals and its effect might be to cause sudden drops in amplitude in some samples. It would thus be obvious for the skilled person to provide the absolute value circuit (56) with means for filtering out samples which are clearly out of range, for instance by ignoring all the samples whose amplitude is much lower than that of the previous samples. Such filtering means would constitute "pattern detecting means" adapted to detect a "specific pattern", the specific pattern being that the amplitude of the detected digital signal is below a certain threshold.

The skilled person would thus arrive at the subject-matter of present claim 1 without having exercised any inventive activity.

4.6 Accordingly, the subject-matter of claim 1 does not involve an inventive step in view of the state of the art disclosed in D2.

5. For the above reasons the appellant's request is not allowable.

## Order

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar: The Chairman:

D. Sauter F. Edlinger