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Datasheet for the decision of 8 November 2006

Case Number: T 1386/04 - 3.5.02

Application Number: 96920317.3

Publication Number: 0829135

IPC: H03H 11/18

Language of the proceedings: EN

Title of invention:
Phase shifting circuit and method for providing a phase shift

Patentee:
Rambus Inc.

Opponent:
Micron Europe Ltd.

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
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Case Number: T 1386/04 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 8 November 2006

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Decision under appeal:
Interlocutory decision of the Opposition Division of the European Patent Office posted 23 August 2004 concerning maintenance of European patent No. 0829135 in amended form.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: M. Ruggiu
E. Lachacinski

Summary of Facts and Submissions

I. This is an appeal of the opponent against the interlocutory decision of the opposition division concerning the maintenance of European patent No. 0 829 135 in amended form.

The opposition division found that the subject-matter of claim 1 of the patent in suit as granted and of an amended claim 1 in accordance with a first auxiliary request lacked novelty, whereas it considered that the subject-matter of claim 1 in accordance with a second auxiliary request met the requirements of the EPC.

II. The second auxiliary request approved by the opposition division comprises eight claims, of which claim 1 reads as follows:

"A phase shifting circuit (200, 500) comprising:

a) a triangle wave generator (201) coupled to receive an input reference signal (CLK), the triangle wave generator (201) including

a1) a pair of complementary outputs (A, B) that output a pair of complementary triangle wave signals (VOUT, VOUTB) of opposite polarity in response to the input reference signal (CLK),

a2) a filter (203) comprising a capacitor (220) coupled across the complementary outputs (A, B), and

a3) a current switch (202) coupled to receive the input reference signal (CLK), the current switch (202) providing an output current (IOUT) at the complementary outputs

(A, B) and comprising:

- a first input coupled to the input reference signal (CLK);
- a second input coupled to a complementary input reference signal (CLKB);
- a first field effect transistor (FET) (302) including a gate coupled as the first input of the current switch (202), a first terminal coupled as a first one (A) of the complementary outputs (A, B) of the current switch (202), and a second terminal coupled to a first node;
- a first current source (306) coupled between a first supply rail (VCC) and the first terminal of the first FET (302);
- a second FET (304) including a gate coupled as the second input of the current switch (202), a first terminal coupled as a second one (B) of the complementary outputs (A, B) of the current switch (202), and a second terminal coupled to the first node;
- a second current source (308) coupled between the first supply rail (VCC) and the first terminal of the second FET (304); and
- a third current source (305) coupled between the first node and a second supply rail (VSS);

wherein the current switch (202) reverses a direction of flow for the output current (IOUT) in response to the input reference

signal (CLK), the filter (203) integrating the output current (IOUT) to result in said complementary triangle wave signals (VOUT, VOUTB);

the phase shifting circuit (200, 500) further comprising:

b) a comparator (205, 505) having a pair of inputs (+, -) coupled to receive the pair of complementary triangle wave signals (VOUT, VOUTB) of opposite polarity, the comparator (205, 505) detecting crossing points of said complementary triangle wave signals (VOUT, VOUTB) and outputting an output clock signal (Q) transitioning in response to detection of the crossing points wherein the output clock signal (Q) includes a predetermined phase relationship with respect to the input reference signal (CLK) in response to a comparison between the pair of complementary triangle wave signals (VOUT, VOUTB)."

Claims 2 to 7 are dependent on claim 1. Claim 8 is an independent claim defining a method for providing a phase shift between an output clock signal (Q) and an input reference signal (CLK).

III. The following prior art documents cited in the statement of grounds of appeal are relevant to the present decision:

D1: US-A-4 866 397 and

D3: "Systematic Distortion Analysis for MOSFET Integrators with Use of a New MOSFET Model" by Gert Groenewold and Waldemar J. Lubbers, published

in IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 41, No. 9, September 1994, pages 569 to 580.

IV. Oral proceedings before the board took place on 8 November 2006. As announced in a fax received at the EPO on 6 November 2006, the patent proprietor was not represented at the oral proceedings.

The appellant (opponent) requested that the decision under appeal be set aside and that the European patent No. 0 829 135 be revoked.

The board noted that the respondent (patentee) had requested in writing that the appeal be dismissed.

V. As regards claim 1, the appellant essentially argued as follows:

The phase shifting circuit of Figure 3 of document D1 included a differential pair of bipolar junction transistors (BJTs) 26, 28 controlled by an input voltage signal Vin applied to their bases. The input voltage signal Vin was a square wave signal centred about a threshold voltage level and made the first and second transistors 26, 28 alternatively conductive and non-conductive. The transistor channels were coupled between respective resistors 32, 34 of equal resistances R and a common constant current source 30 and thence to ground. The resistors 32, 34 were coupled at their other ends to a supply voltage Vcc. A capacitor 36 of capacitance C was connected across the transistor-resistor junctions, which junctions were also coupled to a limiter 54 shown schematically in

Figure 2 of D1. Claim 1 as approved by the opposition division called for first and second current sources, which the opposition division interpreted as meaning constant current sources rather than an arrangement of elements which together acted to provide a substantially constant source of current as in D1. However, the wording of claim 1 did not require constant current sources but merely sources of current, and D1 satisfied this feature of claim 1 because an analysis of the circuit of Figure 3 showed that, when the time constant RC was large (as was disclosed in D1), substantially constant currents flowed in the resistors 32, 34. In any case, it was obvious to the skilled person to use constant current sources instead of the resistors 32, 34 in an integrator circuit of the type shown in Figure 3 of D1. This was in particular apparent from the integrator circuits shown in Figures 3(b) and 19(b) of document D3. These prior art circuits used FETs as switching transistors so that it was also obvious to the skilled person in view of D3 to replace the BJTs of the circuit shown in Figure 3 of D1 by FETs. D3 mentioned as applications of the circuits described there video circuits, audio circuits, intermediate-frequency filters, and disk-drive read channels. TV/video circuits in particular had to be able to process frequencies of up to at least 5.5 MHz and thus were suited for use at the frequencies envisaged in D1 (column 2, lines 5 to 7). The opposition division was right in considering that FETs and BJTs were functional equivalents and always obviously interchangeable unless under very special circumstances and that in D1 the choice of transistor was particularly unrestricted because the switching transistors of D1 were driven by digital clock signals,

which made the circuit insensitive to any offsets due to large and/or varying threshold voltages in FETs or Vbe in BJTs, and because the constant current source 30 generated the current switched by the transistors, whereby the voltage drop across the collector/emitter or drain/source path of the conducting transistor was of no importance. The circuit of Figure 3 of D1 was symmetrical and had been analysed assuming the current drawn by the limiter 54 from the transistor-resistor junctions and the channel resistance of the transistors 26, 28 were both negligible. The analysis showed that the circuit had a stable dynamic steady state. With the time constant RC being large, the voltages on the two terminals of capacitor 36 were substantially complementary triangle waves of equal peak-to-peak amplitudes, as in the patent in suit. Because the circuit was symmetrical, the complementary triangle waves crossed in the middle of their peak-to-peak excursions (i.e. had opposite polarities) at quadrature phase with respect to the input voltage signal Vin. No specific form of limiter was individualised in relation to Figure 3 of D1. However, Figure 4 of D1 illustrated a phase-shifting circuit that used a differential amplifier as a limiter 54 having the same function as the limiter 54 of Figure 2. It was apparent that this differential amplifier was driven to saturation when one of the signals at its output was greater than the other. Thus, the differential amplifier 54 of Figure 4 of D1 was in fact a comparator. At the very least, it was obvious to the skilled person that the differential amplifier of Figure 4 was suitable to form the limiter 54 of Figure 2 of D1. Therefore, the subject-matter of claim 1 as approved by the opposition division did not involve an inventive step.

VI. The arguments of the respondent can be summarised as follows:

Each calculation step given by the opponent in its analysis of the circuit of Figure 3 of D1 was carried out in view of the final result the opponent sought to achieve. Document D1 related essentially to a wide band adjustable phase shifter shown in Figure 4 and the only significant statement relating to the phase shifter shown in Figure 3 was a short description of the components followed by the conclusion that the output signal of the circuit was an RC exponential signal that was provided to the limiter 54 of Figure 2. The skilled artisan would not set up equations to acquire an understanding of how the circuit of Figure 3 of D1 worked and, according to the skilful understanding, the circuit of Figure 3 of D1 was not an adequate means to produce a triangular waveform. The analysis presented by the opponent of the circuit shown in Figure 3 of D1 led, under the assumption of a large time constant RC, to the elimination of RC from the equations and to a constant current in the resistors 32, 34. However, there was no incentive to use current sources instead of the resistors of D1. The resistors 32, 34 constituted the load of the differential pair shown in Figure 3 of D1 and accordingly did not represent a source at all. In order to understand the resistors as a current source, the step from the resistor's load functionality to the source functionality was to be carried out beforehand. However, document D1 did not give any incentive to make the step from load to source and there was no general tendency to replace loads by sources. D1 indicated clearly that the outputs of the

circuit shown in Figure 3 were exponential. D1 referred to large time constants by the following terms: "By using a large time constant (e.g. by using a large capacitance), signal 18 becomes almost linear in the region of interest in Fig. 1....". Accordingly, signal 18 of Figure 1 was not related to the circuit shown in Figure 3. The region of interest was a section of signal 18 where the signal dropped across a threshold level. However, when signal 18 reached the lowest level, it remained constant for a certain amount of time. After this little pause, the signal rose according to an exponential slope. Even if the rising and falling slopes would be assumed to be strictly linear (an assumption that was not shown in Figure 1 of D1) the overall waveform would not be triangular because of the flat section on the bottom of the signal. Moreover, signals 18 or 12 of Figure 1 were always single ended and the limiter 54 in Figure 2 of D1 was represented as a block with one single input. Thus, the input to the limiter was not two complementary triangular signals. Consequently, D1 failed to disclose a triangular waveform generator with two current sources and it did not even disclose complementary triangular waveforms. D1 disclosed bipolar transistors and failed to disclose MOSFETs as components for the input differential pair. Beside the tendency for certain types of circuitries, there was no general movement to replace all bipolar circuitry by MOSFET. Particularly for high speed and low noise applications, as for example phase shifting circuits, experts were rather reluctant to integrate MOSFETs. This was due to the comparably low speed and high noise level of MOSFETs at the priority date. Additionally, MOSFETs were susceptible to substrate noise, thermal coupling and high offset voltages. So,

even if the skilled person considered replacing the bipolar transistors by respective MOSFETs, the resulting circuitry would suffer from numerous imperfections. The strategy to overcome the problems was disclosed in the patent in suit and resided in triangular waveform generators, current sources and comparators, all being arranged to produce and process two complementary triangular waveforms. The limiters 54 of Figures 2 or 4 of D1 were not comparators and they did not have the same technical effect as a comparator, even under the assumption of an input of two complementary triangular waveforms. The limiter 54 shown in Figure 4 of D1 determined the difference of the two input signals N4 and N3 resulting in a signal V4,3 that was then limited according to a reference value Vref. During normal operation, the reference voltage Vref was assumed to coincide with zero (here half-way between Vcc and Vss) so that the limiter produced high and low values of equal lengths at an output N5. However, when process, supply or temperature variations or other noise sources existed, the reference voltage Vref varied with respect to its nominal value of zero and the lengths of the periods in which the output N5 was low and high differed from each other. By contrast the result of a comparison between the two signals N4 and N3 was independent from their common levels with respect to zero, or with respect to any threshold value. Therefore, D1 failed to disclose a comparator. Document D3 related to a distortion analysis of MOSFET integrators and presented a new model for the MOSFET. D3 belonged to the technical area of audio signal processing and lacked the slightest technical relation to phase shifting circuits. The rather slow (low frequency of audio signals, max. 20

kHz) and distortion free circuits disclosed in D3 were irrelevant for the high frequency applications (approx. 250 MHz) of the invention of the patent in suit. Further, D3 failed to show complementary triangular waveforms being fed to a comparator. Thus, even if by coincidence, the skilled artisan would consider the combination of D3 and D1, this would not result in the subject-matter of claim 1.

Reasons for the Decision

1. The appeal is admissible.

2. D1 is a prior art document that relates to phase shifters. In Figure 3, D1 shows a phase shifter comprising a current switch with a first input 22 coupled to receive an input reference signal and a second input 24 coupled to receive a complementary input reference signal. The current switch shown in Figure 3 of D1 comprises a first switching transistor 26 of the bipolar junction type (BJT). Transistor 26 includes a base coupled as the first input of the current switch, a first terminal coupled as a first one 40 of complementary outputs of the current switch and a second terminal coupled to a first node. A first resistor 32 is coupled between a first supply rail Vcc and the first terminal of the first transistor 26. A second switching transistor 28 includes a base coupled as the second input of the current switch, a first terminal coupled as a second one 38 of the complementary outputs of the current switch and a second terminal coupled to the first node. A second resistor 34 is coupled between the first supply rail

Vcc and the first terminal of the second transistor 28. A current source 30 is coupled between the first node and ground, which forms a second supply rail. A filter comprising a capacitor 36 is coupled across the complementary outputs 38, 40. It is apparent from Figure 1 of D1 that the input reference signal and the complementary input reference signal are square waves of 50% duty cycle. Thereby, the transistors 26 and 28 are controlled so as to be alternatively conductive and non-conductive and the current switch reverses a direction of flow for the output current in capacitor 36 in response to the input reference signal. The capacitor 36 of the filter integrates the output current of the current switch. Column 1, lines 63 to 65 of D1 states that the output signal is an RC exponential signal. However, a passage from column 1, line 65 to column 2, line 3 of D1 indicates that obtaining a 90° phase shift requires that a large time constant be used, whereby the output signal 18 becomes almost linear in the region of interest in Figure 1. In the statement of grounds of appeal, the appellant has provided an analysis of the circuit of Figure 3 for the case that the time constant RC is large, as proposed in D1. This analysis has convinced the board that, with a large time constant, the voltages on the two ends of capacitor 36 are substantially complementary triangle waves of equal peak-to-peak amplitudes and thus of opposite polarities. It appears therefore that the current switch of Figure 3 of D1 includes a triangle wave generator whose outputs on terminals 38, 40 are complementary triangle wave signals. According to D1, column 1, lines 62 to 64, the output signal on the terminals 38, 40 is provided to a limiter 54 of Figure 2. It is apparent that this limiter 54 provides

an output in the form of a square wave signal (see Figure 1 of D1). Where the phase shift is 90°, the output of the limiter is thus an output clock signal that includes a predetermined phase relationship with respect to the input reference signal. From said analysis of the circuit of Figure 3 of D1, it further appears that, when a large time constant is used, the currents in resistors 32 and 34 are substantially constant currents of equal values (which results in substantially linear, complementary triangle wave signals on terminals 38, 40).

3. Claim 1 of the patent in suit specifies current sources, not constant current sources. The board considers that in its general meaning the term "current source" designates an element that sources, i.e. delivers a current, not necessarily an element that delivers a definite constant current whose value is substantially independent of the value of the load or the value of the voltage to which the element is connected. Therefore, the board considers that the circuit of Figure 3 of D1 includes a first current source coupled between the first supply rail Vcc and the first terminal of the first switching transistor 26, and a second current source coupled between the first supply rail Vcc and the first terminal of the second switching transistor 28.

4. The novelty of the subject-matter of claim 1 of the patent in suit is not in dispute.

The switching transistors of the circuit of Figure 3 of D1 are bipolar junction transistors (BJTs). Thus, the subject-matter of claim 1 of the patent in suit differs

from this prior art in that the switching transistors are field effect transistors (FETs).

D1 indicates that the output signal on terminals 38, 40 is provided to a limiter 54 of Figure 2. However, D1 does not provide further details of the limiter 54 of Figure 2. Thus, the subject-matter of claim 1 of the patent in suit is considered to further differ from the prior art circuit disclosed in D1 in that it comprises a comparator having a pair of inputs coupled to receive the pair of complementary triangle wave signals of opposite polarity, the comparator detecting crossing points of said complementary triangle wave signals and outputting the output clock signal transitioning in response to detection of the crossing points so that the phase relationship of the output clock signal with respect to the input reference signal is in response to a comparison between the pair of complementary triangle wave signals.

5. In view of the data rates (2 megabit/second and 1.544 megabit/second) mentioned at column 2, lines 5 to 7 of D1, the board considers that it is obvious to the skilled person that FETs are a suitable alternative to BJTs as switching transistors in the current switch of Figure 3 of D1. This is confirmed by document D3 which discloses integrator circuits using MOSFETs. D3 refers to video circuits in its introduction, and thereby to frequencies of up to at least 5.5 MHz. In particular, the circuit shown in Figure 19(b) of D3 comprises a differential pair of MOSFETs.

6. Figure 4 of D1 shows an element 54 having two inputs receiving signals N4, N3 present at the ends of a

capacitor. From the waveforms V4,3 and N5 of Figure 5 of D1, it is apparent that the output N5 of the element 54 saturates at a high value when the difference V4,3 of the signals N4, N3 at its inputs is higher than a threshold 74 and at a low value when the difference V4,3 is lower than the threshold 74. According to column 4, lines 15 to 17 of D1, the element 54 of Figure 4 can be a differential amplifier and, in this case, the threshold value will be 50 percent of the peak-to-peak value. D1 does not show any other input signal than the signals N4 and N3 to the differential amplifier 54 of Figure 4. In the view of the board, this means that the differential amplifier 54 of Figure 4 of D1 effectively compares the signals N4, N3 at its inputs, i.e. detects crossing points of the signals N4, N3, and output a signal transitioning in response to detection of the crossing points.

7. The differential amplifier 54 shown in Figure 4 of D1 has the same function as the limiter 54 of Figure 2, namely to convert the signal at its input into a square wave signal. Therefore, it is obvious to the skilled person that the limiter 54 of Figure 2 of D1 can take the form of a differential amplifier as in the circuit of Figure 4. When a differential amplifier is used in conjunction with a large time constant for the circuit of Figure 3 of D1, the phase relationship of the output clock signal with respect to the input reference signal is in response to a comparison between the pair of complementary triangle wave signals.

8. Thus, having regard to the state of the art, the subject-matter defined by claim 1 of the patent in suit is obvious to a person skilled in the art and does not

involve an inventive step in the sense of Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The patent is revoked.

The Registrar: The Chairman:

U. Bultmann W. J. L. Wheeler