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Datasheet for the decision
of 10 September 2008

Case Number: T 0132/06 - 3.4.03

Application Number: 98116103.7

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Language of the proceedings: EN

Title of invention:
Field emission electron source, method of producing same, and use of the same

Applicant:
MATSUSHITA ELECTRIC WORKS, LTD.

Opponent:
-

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 54, 56, 83, 113(1)

Keyword:
"Novelty (no) - main and second auxiliary request"
"Inventive step (no) - first and third auxiliary request"
"Sufficiency of disclosure - fourth auxiliary request - remittal for further prosecution"

Decisions cited:
-

Catchword:
-

Case Number: T 0132/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 10 September 2008

Appellant: MATSUSHITA ELECTRIC WORKS, LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 8 August 2005 refusing European application No. 98116103.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: R. Q. Bekkering
J. Van Moer

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 98 116 103 for lack of novelty, Article 54(1), (2) EPC 1973, over

D1: EP 0 798 761 A.

II. At oral proceedings before the board the appellant applicant requested that the decision under appeal be set aside and that a patent be granted in the following version:

main request: the claims as refused;
first and second auxiliary request as filed with the statement of the grounds of appeal;
third auxiliary request as filed in August 2008;
fourth auxiliary request submitted during oral proceedings.

Furthermore, as a fifth, procedural request, remittal to the department of first instance for further prosecution was requested.

III. Claim 1 of the main request reads as follows:

*"A field emission electron source comprising:
an electrically conductive substrate (1, 2);
a porous polysilicon layer (6) formed on the surface of said electrically conductive substrate (1, 2) on one side thereof and having nanostructures; and
a thin metal film (7) formed on said porous polysilicon layer (6), wherein a voltage is applied to said thin metal film (7) used as a positive electrode with*

respect to said electrically conductive substrate (1, 2) thereby to emit an electron beam through said thin metal film (7),
characterized in that
said porous polysilicon layer (6) is a polycrystal having grains and that the nanostructures have an oxidized or nitrided coating thereon on the surface of the grains".

IV. Claim 1 of the first auxiliary request reads as follows:

"A field emission electron source comprising:
an electrically conductive substrate (1, 2);
a porous polysilicon layer (6) formed on the surface of said electrically conductive substrate (1, 2) on one side thereof and having nanostructures; and
a thin metal film (7) formed on said porous polysilicon layer (6), wherein a voltage is applied to said thin metal film (7) used as a positive electrode with respect to said electrically conductive substrate (1, 2) thereby to emit an electron beam through said thin metal film (7),
wherein said porous polysilicon layer is an oxidized or nitrided porous polysilicon layer (6),
characterized in that
said polysilicon layer (6) is an undoped polysilicon layer".

V. Claim 1 of the second auxiliary request consists of the pre-characterising portion of claim 1 of the first auxiliary request and the following characterising portion:

"characterized in that
said porous polysilicon layer (6) is made by alternately laminating a polysilicon layer having high porosity and a polysilicon layer having low porosity".

VI. Claim 1 of the third auxiliary request corresponds to claim 1 of the main request with the following addition at the end of the claim:

"the surface of the grains being made porous and the core of the grains retaining a crystal state".

VII. Claim 1 of the fourth auxiliary request corresponds to claim 1 of the second auxiliary request with the following characterising portion:

"characterized in that
said porous polysilicon layer (6) is made by alternately laminating a polysilicon layer (4b) having high porosity and a polysilicon layer (4a) having low porosity,
wherein said porous polysilicon layer (6) is a layer whose porosity changes in a direction of thickness so that said porosity is higher on a side of the electrically conductive substrate (1, 2) than on a front surface side".

VIII. Furthermore, all claim requests include a claim for a method of producing the field emission electron source of claim 1.

IX. The appellant applicant argued as follows:

The subject-matter of claim 1 of the main request was new over document D1. Admittedly document D1 disclosed polysilicon as a possible alternative to the monocrystalline material used for the semiconductor layer. However, the provision of an oxidised or nitridised coating on the porous semiconductor layer, if any, was only disclosed in the embodiment using monocrystalline material. It was not legitimate to combine different embodiments from D1 to construct a novelty-destroying disclosure.

The subject-matter of claim 1 of the first auxiliary request was new and inventive over D1, which neither disclosed nor suggested the use of undoped polysilicon.

As regards the second auxiliary request, the subject-matter of claim 1 was new and inventive over D1, which did not suggest a low porosity polysilicon layer at the surface overlying a high porosity polysilicon layer. This resulted in a highly efficient and stable electron emission, which could not be achieved with a conventional field emission electron source based on single-crystal silicon with a porous surface, as known from D1.

As far as the third auxiliary request was concerned, the features that the surface of the grains were made porous and the core of the grains retained a crystal state had the advantage that the heat generated by applying the voltage was transmitted along the crystal and radiated to the outside. The temperature rise of the porous polysilicon layer was thus smaller than that

of a single crystal silicon layer, providing a more stable electron emission current.

Finally, claim 1 of the fourth auxiliary request, in contrast to that of the second auxiliary request, explicitly required the porosity on the substrate side to be higher than that at the front surface. As argued for the second auxiliary request, this resulted in a more efficient and stable electron emission.

Responding to the board's objection that it was not apparent from the application documents how such a structure could be obtained, the applicant appellant requested the opportunity to submit evidence to this effect and requested that the case be remitted to the department of first instance for further prosecution.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Novelty*

Document D1 discloses, using the terminology of claim 1, a field emission electron source comprising:
an electrically conductive substrate (10, 11);
a porous polysilicon layer (14) formed on the surface of said electrically conductive substrate on one side thereof and having nanostructures; and
a thin metal film (15) formed on said porous polysilicon layer, wherein a voltage is applied to said

thin metal film used as a positive electrode with respect to said electrically conductive substrate thereby to emit an electron beam through said thin metal film, as per claim 1 of the main request (see figure 1 and corresponding description of D1).

In particular, in D1 "*the porous semiconductor layer 14 is formed in the semiconductor layer 12 through the anodic treatment*" (column 3, lines 54, 55). Moreover, "*a crystalline, amorphous, poly-crystalline, n-type or p-type Si layer may be used through the anodization*" (column 4, lines 37, 38). Accordingly, D1 discloses the formation by anodisation of a porous poly-crystalline silicon layer. Hence the layer has nanostructures (separating the pores) of poly-crystalline silicon which have grains.

Furthermore, in D1 "*to stabilize the porous Si layer 14, the element-substrate 10 is put into the vacuum heating to remove such hydrogen terminations and then carried to the heating condition in an oxygen and nitrogen gaseous atmosphere to form -O or -N terminations instead of the hydrogen terminations. Alternatively, this replacement of the O or N termination may be performed by the plasma treatment under the oxygen and nitrogen gaseous condition*" (column 5, line 58 to column 6, line 8). Accordingly, the nanostructures will have "*an oxidized or nitrided coating thereon on the surface of the grains*" as specified in claim 1.

The applicant appellant's argument that the above-mentioned disclosure in D1 related solely to the embodiment using monocrystalline silicon for the semiconductor layer 12 has not persuaded the board. It

is indeed correct, as argued by the appellant, that where a prior art document discloses different distinct embodiments, a *per se* undisclosed combination of individual features taken from different embodiments in general cannot be held prejudicial to the novelty of a claim directed at such a combination. However, prior art documents commonly contain a description of an embodiment including the mention of possible alternatives at various stages, in which it is implicit that, unless specified otherwise, the alternatives are interchangeable and the subsequent description in principle applies to any of these alternatives although the description, by way of example or preference, confines itself to one alternative. This is merely a conventional and efficient way of describing what are in effect many embodiments, thereby avoiding undue repetition. This is the case in D1. After listing a number of alternatives to monocrystalline silicon, including poly-silicon, for the semiconductor layer 12 (column 4, lines 37-38), the description continues with the manufacturing process employing single-crystal silicon. It is nevertheless implicit for the skilled reader that the same process is intended for the other materials.

Hence, having regard to D1, the subject-matter of claim 1 of the main request is not new (Article 54(1) and (2) EPC 1973).

Accordingly, the main request falls to be refused.

3. *First auxiliary request*

3.1 *Novelty*

According to document D1, an n-type or p-type silicon layer may be used (column 4, lines 37, 38). Undoped silicon is not mentioned.

Hence, the subject-matter of claim 1 of the first auxiliary request is new over D1 (Article 54(1) and (2) EPC 1973).

3.2 *Inventive step*

The anodic treatment in the HF solution to form the pores requires a supply of holes at the exposed surface of the silicon layer. Whereas these holes are available in sufficient quantity in p-type Si, exposure of the silicon layer to light is necessary to provide these holes in case of n-type silicon (column 3, line 54 to column 4, line 22). Moreover, according to D1 a porous layer having a high resistance is desirable so that most of the electric field is across this layer (column 6, line 41 to column 7, line 3).

In the light of these considerations, it would be obvious to the person skilled in the art to use undoped silicon as an alternative to n-type or p-type doped silicon specified in document D1. This commonly used material has the required high resistivity and would be easily made porous through anodisation by applying the above principles explained in D1.

Accordingly, the subject-matter of claim 1 of the first auxiliary request would be obvious to the person skilled in the art and, therefore, does not involve an inventive step (Article 56 EPC 1973).

Hence, the first auxiliary request falls to be refused.

4. *Second auxiliary request*

4.1 *Novelty*

As disclosed in D1 "*the internal diameter of the minute channel in the surface of the porous Si layer is comparatively large, but such internal diameter of the minute channel gradually decreases as its depth becomes deeper. Thus, the porous Si layer 14 has a high resistivity at a portion adjacent to its surface and a low resistivity at a portion adjacent to its interface between the porous Si layer 14 and the Si layer 12. This incline of resistivity in the porous Si layer 14 is preferable for the injection of electrons from the substrate*" (column 4, lines 50 to column 5, line 1).

It should be noted that "*laminating*" the "*layers*" in claim 1 is to be understood in the sense used throughout the application of forming superposed notional layers within the layer of polysilicon material. In fact, these layers are formed within the polysilicon layer by successive anodisation processes under different conditions (original application, page 17, line 15 to page 18, line 29).

Document D1 discloses a gradual decrease of the pore diameter rather than stepwise in layers.

Hence, the subject-matter of claim 1 of the second auxiliary request is new over D1 (Article 54(1) and (2) EPC 1973).

4.2 *Inventive step*

In the board's judgement, however, it would be obvious to the person skilled in the art that alternatively a decrease of the porosity could be effected in layers given that a sequence of discrete processing steps is practically the rule in the semiconductor art.

Hence, the subject-matter of claim 1 of the second auxiliary request does not involve an inventive step (Article 56 EPC 1973).

Hence, the second auxiliary request also falls to be refused.

5. *Third auxiliary request*

5.1 *Novelty*

Claim 1 of the third auxiliary request differs from that of the main request in that it further specifies: "*the surface of the grains being made porous and the core of the grains retaining a crystal state*".

Polycrystalline silicon is a material consisting of multiple small silicon crystals, ie grains. When exposed to the anodisation process, which both in the application and in D1 is essentially an electrochemical etching process using an HF solution where etching of

the silicon takes place at the silicon/HF solution interface, the surface of the grains will inevitably be etched first so as to form pores therein, leaving the core of the grains unaffected in their crystal state.

Accordingly, for the skilled reader the above additional feature is implicitly disclosed in D1.

Hence, the subject-matter of claim 1 of the third auxiliary request is also not new with respect to document D1 (Article 54(1) and (2) EPC 1973).

Accordingly, the third auxiliary request also falls to be refused.

6. *Fourth auxiliary request*

6.1 Compared to claim 1 of the second auxiliary request, claim 1 of the fourth auxiliary request further specifies that "*said porous polysilicon layer (6) is a layer whose porosity changes in a direction of thickness so that said porosity is higher on a side of the electrically conductive substrate (1, 2) than on a front surface side*".

6.2 Although only filed during the oral proceedings, the request is admitted into the proceedings because it aims to overcome the board's objections against the second auxiliary request by including the additional features of dependent claim 2 of this latter request.

6.3 According to the description (original application, page 17, line 15 to page 18, line 29), the manufacturing process in its simplest form with only

two porous layers (4a and 4b, see figure 10) consists of the following steps, after formation of polysilicon layer 3: a first anodisation process at a first condition (current density of 2.5 mA/cm^2 for 4 seconds) resulting in a porous layer 4a having a low porosity, followed by a second anodisation process at a second condition (current density of 20 mA/cm^2 for 5 seconds) resulting in a porous layer 4b having a high porosity formed on one side of the layer 4a adjacent substrate 1 (page 18, lines 1 to 22).

However it appears to the board that as the anodisation process is essentially an electrochemical etching process using an HF solution in which etching of the silicon takes place at the silicon/HF solution interface, the second anodisation process, while forming pores at a greater depth, ie in layer 4b, would inevitably increase the porosity of layer 4a which would also be exposed to this second electrochemical etching process. Hence, it appears that the porosity of the layer at the front surface would necessarily be higher than that of the layer at the substrate side, contrary to what is specified in claim 1 of the fourth auxiliary request and in the description.

Accordingly, it would appear that the alleged invention is not disclosed in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art (Article 83 EPC 1973).

The above is equally true for the method according to claim 7.

6.4 The appellant applicant traversed this objection of insufficiency stating that, given time, they would be able to produce evidence in support of this traverse. Accordingly they requested that they be given the opportunity to submit this evidence, and that to this end the case be remitted to the department of first instance for further prosecution.

In view of the fact that the issue arose in the course of the oral proceedings, the board considers it appropriate that the appellant be given the opportunity to submit such evidence in order to safeguard their right to be heard (Article 113(1) EPC 1973).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution on the basis of the fourth auxiliary request.

Registrar	Chair
S. Sánchez Chiquero	R. G. O'Connell