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Datasheet for the decision of 9 October 2008

Case Number: T 0427/06 - 3.4.03

Application Number: 97915823.5

Publication Number: 0890184

IPC: H01L 21/00

Language of the proceedings: EN

Title of invention:
A method for producing a semiconductor device having a semiconductor layer of SiC and such a device

Applicant:
CREE, INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 0427/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 9 October 2008

Appellant: CREE, INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 5 January 2006 refusing European application No. 97915823.5 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: G. Eliasson
J. Van Moer

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 97 915 823 for lack of inventive step over the prior art documents

D1: US 5 021 851 A;
D2: GB 1 201 428 A;
D3: GB 1 397 305 A.

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and a patent granted in the following version:

claims 1 to 10 submitted during the oral proceedings;
description pages 1 to 11 submitted during the oral proceedings;
drawings as originally filed.

III. Claim 1 of the above request reads as follows (board's emphasis marking amendments with respect to the refused version):

"1. A method for producing a semiconductor device having a semiconductor layer with at least a pn—junction (7) therein, comprising a step

a) of implanting an impurity dopant of a first conductivity type, being one of a) n and b) p, into said semiconductor layer being doped according to a second opposite conductivity type for forming a first type doped near surface layer (4) in said semiconductor layer and a step

b) of annealing said semiconductor layer at a high temperature for making the implanted impurity dopants electrically active,

characterized in that the semiconductor layer is of crystalline SiC and the combination that in step b) said annealing is carried out at such a high temperature that at least a portion of said dopants diffuses into the non—implanted sub-layer of said semiconductor layer following said near surface layer, **that the annealing temperature is selected to be approximately 1700ºC,** that in step a) first conductivity type impurity dopants of at least two different elements are implanted in the semiconductor layer and that at least one of said elements is slowly diffusing in SiC at said annealing temperature **and implanted at a dose corresponding to a concentration above 10^{19} cm^{-3}** for retaining a high doping of said near surface layer after annealing for making it possible to form a good ohmic contact to said semiconductor layer and at least one of said elements is rapidly diffusing in SiC at said annealing temperature for locating a pn—junction (7) so created at a considerable distance from said near surface layer at a depth being at a considerable distance from the region damaged by the implantation **locating the active pn-junction in an area of high crystalline perfection, that p-type impurity dopants are implanted in said semiconductor layer in step a),**

and that boron is implanted in step a) as said rapidly diffusing element."

IV. The appellant applicant argued essentially as follows:

(a) The claimed method produced a semiconductor device made of SiC with at least one pn-junction located in an area of high crystalline perfection, thereby making it possible to benefit from the excellent properties of SiC.

(b) Although the use of diffusion techniques for forming pn-junctions in SiC was known *per se* in the art, diffusion was considered to be no real option due to the low diffusion coefficients of the possible dopants. The prior art methods known from documents D2 and D3 required temperatures above 2000°C for diffusing boron from a bulk source, temperatures which were incompatible with conventional semiconductor processing.

(c) Document Dl disclosed a method of forming a pn-junction in a crystalline Si layer comprising a step of implantation followed by a step of annealing to cause the implanted dopant to diffuse deeper into the semiconductor layer of Si. It was however known that the diffusion coefficients of most dopants in Si were, in contrast to those for diffusion in SiC, high enough to make diffusion a suitable technique for Si.

(d) The present invention built on the surprising insight that implanted boron diffused much more rapidly than what one would expect from the results based on diffusion from a bulk source. Thus the implantation step unexpectedly made diffusion of boron in SiC possible at typical annealing temperatures, around 1700°C, where diffusion of boron from a bulk source would be negligible.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

Claim 1 is based on claims 1, 3, 5 and 14 as originally filed in combination with the disclosure on page 3, lines 20 to 31 of the application as originally filed. Dependent claims 2 to 10 correspond to renumbered original claims.

The board judges that the requirements of Article 123(2) EPC are met.

3. *Inventive step*

3.1 Document D1 was considered closest prior art in the decision under appeal. It discloses a method of forming a pn-junction in a crystalline Si layer comprising the steps of implanting P and As ions followed by annealing (abstract). Since P has a higher diffusion coefficient in Si than As, it diffuses further into the Si layer beyond the implanted region (column 2, line 44 to column 3, line 57). The result is a graded pn-junction with a highly doped region having a doping concentration of more than 10^{19} cm^{-3} near the surface (Figure 2). This concentration is generally known in the art to be sufficiently high for forming a good ohmic contact to the Si layer.

3.2 The device of claim 1 differs from that of document D1 in that (i) the semiconductor layer is made of crystalline SiC instead of crystalline Si; (ii) the rapidly diffusing element is boron, whereas in the method of document D1 it is phosphorous; and (iii) the annealing temperature is about 1700°C, whereas in the method of document D1 it is about 1000°C (column 3, lines 26 to 33).

3.3 The technical problem relative to document D1 is to increase the high temperature performance of the device produced by the method.

3.4 Because of its large bandgap, SiC is - in theory - a suitable semiconductor material for devices intended to work at high voltages and temperatures where silicon devices would fail (application, page 1, line 30 to page 2, line 8). It is however known to be much more difficult to process than silicon. Firstly, implantation of dopants to form a pn-junction creates crystal defects and whereas in Si these disappear completely on annealing, in SiC they do not. The presence of crystal defects at the pn-junction results in a device having inferior properties, such as reduced breakdown voltage and increased leakage current (application, page 2, lines 24 to 33).

Secondly, the diffusivity of dopants in SiC, such as aluminium and boron, is very low, with the result that conventional diffusion of dopants would have to take place at very high temperatures in excess of 2000°C (item IV(b) above; D2, p6, lines 33 to 37 and 72 to 76; D3, p4, lines 49 to 58).

3.5 Taking the above properties of SiC into account, the board judges that although the skilled person might theoretically and briefly consider the method of document D1 for doping SiC with Al and B in SiC using ion-implantation followed by a step of annealing the substrate, they would assume that the annealing step would have to be carried out at temperatures above 2000°C in order to diffuse boron sufficiently far beneath the implanted region. Because of the very high temperatures involved, this method of forming a pn-junction in SiC would be regarded as of little practical interest.

3.6 The claimed invention builds on the insight that the diffusion coefficient of ion-implanted boron in SiC is greatly enhanced compared to boron diffused in SiC from a bulk source. This enhanced diffusivity makes it possible to reduce the diffusion temperature well below that required for diffusing boron from a bulk source (item IV(d) above).

The skilled person knowing only about the diffusion properties of boron from a bulk source would on the other hand not contemplate carrying out the diffusion step at the claimed temperature of about 1700°C, as no significant diffusion could be expected to take place under these conditions within a reasonable time.

3.7 For the above reasons, in the board's judgement, the subject matter of claim 1 is to be regarded as involving an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   claims 1 to 10 submitted at the oral proceedings;

   description pages 1 to 11 submitted at the oral proceedings;

   drawings as originally filed.

Registrar Chair

S. Sánchez Chiquero R. G. O'Connell