**BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS**

**BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE**

**CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS**

**Internal distribution code:**
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

# Datasheet for the decision of 24 June 2008

**Case Number:** T 0262/07 - 3.5.01

**Application Number:** 97304599.0

**Publication Number:** 0818733

**IPC:** G06F 12/08

**Language of the proceedings:** EN

**Title of invention:**
A multiprocessing system configured to perform software initiated prefetch operations

**Applicant:**
SUN MICROSYSTEMS, INC.

**Opponent:**
-

**Headword:**
Prefetch commands/SUN MICROSYSTEMS

**Relevant legal provisions:**
EPC Art. 123(2)

**Relevant legal provisions (EPC 1973):**
EPC Art. 84, 123(2)

**Keyword:**
-

**Decisions cited:**
G 0002/88

**Catchword:**
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

**Case Number:** T 0262/07 - 3.5.01

# D E C I S I O N
**of the Technical Board of Appeal 3.5.01**
**of 24 June 2008**

**Appellant:** SUN MICROSYSTEMS, INC.
4150 Network Circle
Santa Clara,
California 95054 (US)

**Representative:** Harris, Ian Richard
D Young & Co
120 Holborn
London EC1N 2DY (GB)

**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 11 July 2006 refusing European application No. 97304599.0 pursuant to Article 97(1) EPC 1973.**

**Composition of the Board:**

**Chairman:** S. Steinbrener
**Members:** R. R. K. Zimmermann
G. Weiss

## Summary of Facts and Submissions

I. European patent application No. 97304599.0, publication number EP-A-0 818 733, relates to software initiated prefetching within multiprocessor computer systems.

II. In the examination proceedings, the applicant filed various amendments to the application. In preparation of oral proceedings before the examining division, the applicant filed amended claims on 26 May 2006, independent claims 1 and 12 reading as follows:

"1. A first processing node (12A) comprising:
a local bus (20);
a main memory (22) coupled to said local bus; and
a system interface (24) coupled to said local bus and coupled to said main memory via said local bus, wherein said system interface is configured to initiate a coherency request for a coherency unit upon a network (14) coupled to the system interface, in response to a prefetch command received upon said local bus, to prefetch said coherency unit from a second node via said network to said main memory prior to execution of an instruction that manipulates said coherency unit, and wherein said system interface, upon receipt of said coherency unit provided in response to said coherency request, is configured to transmit said coherency unit upon said local bus,
wherein:
said main memory is configured to receive and to store said coherency unit transmitted by said system interface;
a first said prefetch command comprises a first write transaction upon said local bus having a plurality of

address bits identifying said first write transaction as a prefetch for read access rights to said coherency unit; and
a second said prefetch command comprises a second write transaction upon said local bus having a plurality of address bits identifying said second write transaction as a prefetch for write access rights to said coherency unit."

"12. A method for prefetching a coherency unit into a first processing node (12A)that comprises:
a local bus (20);
a main memory (22) coupled to said local bus; and
a system interface (24) coupled to said local bus and coupled to said main memory via said local bus, said system interface being further coupled to a network, said method comprising:
in response to detecting a prefetch command, received on said local bus within said first processing node, for prefetching a coherency unit from a second node via said network to said main memory prior to execution of an instruction that manipulates said coherency unit, said system interface initiates a coherency request for a coherency unit upon said network;
said system interface receives said coherency unit in response to said coherency request in said first processing node; and
said system interface transmits said coherency unit across said local bus within said first processing node to be stored in said main memory within said processing node,
wherein:
a first said prefetch command comprises a first write transaction upon said local bus having a plurality of

address bits identifying said first write transaction as a prefetch for read access rights to said coherency unit; and
a second said prefetch command comprises a second write transaction upon said local bus having a plurality of address bits identifying said second write transaction as a prefetch for write access rights to said coherency unit."

III. The last two paragraphs defining the first and second prefetch commands were taken unamended from the preceding version of these claims, which had already been the subject of a cautionary advice that "strict support is requested for said paragraphs since they are assumed to be the difference over the prior art in hand" (communication of the examining division dated 15 March 2006, section 1.1).

IV. The examination division refused the application at the oral proceedings held on 28 June 2006 in the applicant's absence, giving the grounds for refusal in writing by letter dated 11 July 2006.

According to the refusal decision, the claims of 26 May 2006 were found to contain added subject matter contrary to Article 123(2) EPC 1973 and to lack clarity contrary to Article 84 EPC 1973. No support could be found in the application as originally filed for the last two paragraphs of the independent claims. The passages cited by the applicant, in particular claims 9 and 10 and the description at page 53, line 24 to page 57, line 4, were worded clearly different from the claims and did thus not support the amendments.

In relation to clarity, the examining division provided an extensive list of different reasons (decision under appeal, section II.3), which may be broadly summarised under two headings: First, the definition of the "prefetch commands" was unclear and their relationship to the "write transactions" could not be understood. Secondly, it was not possible to understand from the claims, the functions and the use of the prefetch operations in the different coherency modes and multiprocessor architectures to which the invention applied. As a last point the list mentions that "the support in the description (Article 84 EPC) for a precise meaning of i) the aliasing in the context of a COMA/NUMA architecture and of ii) the LPA regions and addressing logic involved in the terms LPA region 302, $LPA_{PS}$ region 304 and $LPA_{PM}$ region 306, remains questionable; in particular, the meaning of the acronyms PS, PM and no acronym attached to LPA should be commented, whereas a clear statement on the mode of operation of the prefetch commands (NUMA or COMA) is requested."

In a section of the decision titled " III. Additional Comments", the examining division stated that "no further examination could be carried out in view of the above objections", but nevertheless commented negatively on novelty and inventive step, citing its previous communications.

V. On 7 September 2006, a notice of appeal was filed by the applicant (appellant) against the refusal of the application, including a debit order for payment of the appeal fee. A written statement setting out the grounds of appeal was filed on 16 November 2006.

VI. In a communication annexed to the summons to oral proceedings requested by the appellant on an auxiliary basis, the Board summarised the results of the preliminary examination of the appeal and expressed doubts regarding the admissibility of some of the amendments under scrutiny.

VII. On 30 May 2008, in response to the communication of the Board, the appellant filed amended claims, which are the basis of the present decision. The amendments were confined to the respective two last paragraphs of the independent claims 1 and 12, replacing the expression "a plurality of address bits" by "most significant address bits". The amended passages of claims 1 and 12 read as follows:

"a first said prefetch command comprises a first write transaction upon said local bus having most significant address bits identifying said first write transaction as a prefetch for read access rights to said coherency unit; and
a second said prefetch command comprises a second write transaction upon said local bus having most significant address bits identifying said second write transaction as a prefetch for write access rights to said coherency unit."

VIII. The appellant requested that the decision under appeal be set aside and the case be remitted on the basis of the amended claims to the first instance for expedited consideration of the questions of patentability at the earliest possible opportunity. For the event that these

requests were not allowed, the appellant maintained its request for oral proceedings.

IX. In its written submissions, the appellant expressly disagreed with the examining division in that the claims should be restricted to any specific embodiment or memory organisation like the NUMA or COMA architecture. Citing various parts of the original application, including in particular col. 5, line 50 to col. 7, line 13 and col. 29, line 9 to col. 31, line 27, the appellant argued that there was a clear and unequivocal basis for the claim definitions in the application as originally filed.

Regarding the clarity objections, the appellant complained that it was rather the reasoning of the examining division than the subject matter of the claims which was unclear. The write commands effectively formed an encoding of a prefetch command using write addresses, obviating the need to provide separate prefetch command codes for identifying the prefetch as being for read access rights or write access rights. The prefetch commands were formed by, i.e. they comprised, the write transaction as defined in the claims and disclosed in the application.

The appellant also submitted that the examining division committed a substantial procedural violation, since they raised the objections of lack of clarity for the first time in the decision under appeal. Finally, in view of the age of the application, expedited prosecution of the appeal was requested.

X. After consideration of the amendments submitted, the Board decided to cancel the oral proceedings and to issue the decision on the appeal in writing.

## Reasons for the Decision

1. The appeal is admissible. Moreover, on the basis of the present requests, the decision under appeal must be set aside.

*Clarity (Article 84 EPC 1973)*

2. The requirement of clarity is met if the wording of the claims allows the protection conferred by the patent to be determined and a comparison with the prior art to be made to ensure that the claimed invention is *inter alia* novel (see decision G 2/88 - Friction reducing additive/ MOBIL OIL III, OJ EPO 1990, 93, sections 2 to 2.5 and 7).

3. In the present case, the main points of objection were the terms "prefetch command" and "write transaction" as used in particular in the last two paragraphs of the independent claims and their functions within a multiprocessing systems. However, there are various popular types of such a system already known in the prior art as acknowledged in the introductory part of the description. The terminology of present claims stay within the normal usage of terms used in the field of computer technology and, where a more specific meaning is applied, the application gives an explicit explanation, e.g. for the term "prefetching" in column 6, lines 39 ff. The application does not pose any

relevant problems in understanding the invention and construing the claims.

4. More specifically, claim 1 (as well as claim 12) defines the prefetch command as a signal received upon the local bus and causing the system interface to initiate a coherency request for a coherency unit upon a network coupled to the system interface. Since the term "prefetching" refers to accessing a coherency unit (see also col. 6, line 39 ff.), the term "prefetch command" implies more than a simple "write transaction". The definition "said prefetch command comprises ... write transaction" is thus appropriate and does not justify clarity objections in the present context.

The "sequence" of the first and second prefetch commands has no particular significance within the teaching of the present invention. The claims, and the description, simply refer to two variants of the prefetch command, the one initiates a prefetch for read access rights, the other for write access rights to the coherency unit.

5. The claim definitions are also supported by the description. According to the description, the "computer system defines a write transaction having a certain encoding as a prefetch command" (col. 3, lines 12 to 14). Similarly at col.6, lines 18 to 22: "In one embodiment, the prefetch command is a write stream operation having an address within a predefined address range. The predefined address range indicates that the operation is a prefetch operation" .

According to col. 6, lines 45 to 47, the prefetch command "is a transaction upon a bus (such as SMP bus 20) which causes a prefetch to occur. The command may be performed in response to a prefetch instruction which is executed by a processor 16".

6. In summary, there is no reason to doubt that the definitions of the first and second prefetch commands and of the write transactions are sufficiently clear and unequivocal to allow a comparison with the prior art and an assessment of the scope of protection. The respective objections raised in the decision under appeal are unfounded.

*Added subject matter (Article 123(2) EPC)*

7. The amended claims meet the requirements of Article 123(2) EPC.

8. The examining division did not raise any objections of added subject matter to the claim definitions previous to the last two paragraphs, nor does the Board raise any such objections.

9. The last two paragraphs define first and second prefetch commands which comprise a first and second, respectively, write transaction upon the local bus (see also original claims 9 and 10), their most significant address bits identifying the different types of prefetch, namely for read and write access rights to the coherency unit.

The application as originally filed explicitly discloses two types of prefetch having different access

rights (see for example original claims 3 and 6). The implementation of different prefetch types in the multiprocessing system is disclosed in fig. 14 f. and the corresponding section "Software Prefetch" of the description (see col. 29 ff.).

As indicated generally in the first paragraph of the section, an address space identifies storage locations, but may also "assign additional properties to certain addresses within the address space". According to the embodiment described, addresses having a predefined pattern of the most significant address bits (MSB) are assigned the additional property that write operations to such addresses cause a prefetch requesting read or write access rights depending on the MSB pattern.

These are essentially the features of the last two paragraphs of the amended independent claims. The global objection of added subject-matter as raised by the examining division is thus unfounded.

*Procedural violation*

10. The appellant submitted that the objections under Article 84 EPC 1973 were raised for the first time in the decision under appeal, which constituted a substantial procedural violation. Indeed, the examining division did not explicitly raise any Article-84-objections against the version of the claims on which the application was later refused *inter alia* for lack of clarity, contrary to the procedural requirements of the EPC.

However, it is also apparent from the communication of 15 March 2006, in particular sections 1.1 to 1.2, that the examining division had serious difficulties in understanding and construing the terms of the claims. The appellant should thus not have been taken by surprise that such difficulties developed to fully fledged clarity objections in the oral proceedings, which the appellant did deliberately not attend.

Furthermore, the examining division refused the application for the primary ground of added subject matter. It seems thus unlikely that the procedural irregularity in raising the clarity objection had any direct effects on the outcome of the first instance proceedings, namely the refusal of the application. Under these circumstances, the present shortcomings of the procedure do not amount to a substantial procedural violation.

*Remittal*

11. As follows from the communication dated 15 March 2006 (see point III above), the examining division considered the subject matter of the last two paragraphs of claims 1 and 12 as a potentially inventive contribution over the prior art. The observations made in section III of the decision under appeal, stating that given the understanding of the invention there might be lack of novelty, are put under question marks and subject to the proviso that "no further examination could be carried out in view of the above objections", i.e. the objections concerning clarity and added subject matter. The Board concludes therefrom that a full examination on the merits of the

invention has not yet taken place. The proceedings, therefore, should be continued in first instance with respect to the remaining patentability requirements on the basis of the present claims.

In view of its age, the case should be given priority.

## Order

## For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the examining division for further prosecution on the basis of the claims filed by letter dated 30 May 2008.

The Registrar: The Chairman:

T. Buschek S. Steinbrener