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Datasheet for the decision of 26 November 2010

Case Number: T 0486/07 - 3.5.05

Application Number: 00304366.8

Publication Number: 1058406

IPC: H04L 25/03

Language of the proceedings: EN

Title of invention:
Method and apparatus for reducing the computational complexity and relaxing the critical path of reduced state sequence estimation (RSSE) techniques

Applicant:
LUCENT TECHNOLOGIES INC.

Headword:
Processing intersymbol interference with RSSE/LUCENT

Relevant legal provisions:
EPC Art. 56, 84, 123(2)
RPBA Art. 15(3)

Relevant legal provisions (EPC 1973):
EPC Art. 106, 107, 108

Keyword:
"Support by the description (no) - main and first auxiliary request"
"Clarity (no) - second auxiliary request"
"Clarity and inventive step (no) - third auxiliary request"

Decisions cited:
J 0010/07, T 1129/97

Catchword:
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Case Number: T 0486/07 **-** 3.5.05

D E C I S I O N
of the Technical Board of Appeal 3.5.05
of 26 November 2010

Appellant: LUCENT TECHNOLOGIES INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 19 October 2006 refusing European patent application No. 00304366.8 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: A. Ritzka
Members: M. Höhn
F. Blumer

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division, dispatched 19 October 2006, refusing European patent application No. 00304366.8 because of lack of clarity (Article 84 EPC 1973) and lack of novelty (Articles 52(1) EPC and 54(2) EPC 1973) having regard to the disclosure of

D1: LEE W U ET AL: "A MAXIMUM-LIKELIHOOD SEQUENCE ESTIMATOR WITH DECISION-FEEDBACK EQUALIZATION", IEEE TRANSACTIONS ON COMMUNICATIONS, IEEE INC. NEW YORK, US, vol. 25, no. 9, 1 September 1977 (1977-09-01), pages 971-979, ISSN: 0090-6778, or
D2: CHEVILLAT P R ET AL: "DECODING OF TRELLIS-ENCODED SIGNALS IN THE PRESENCE OF INTERSYMBOL INTERFERENCE AND NOISE", IEEE TRANSACTIONS ON COMMUNICATIONS, IEEE INC. NEW YORK, US, vol. 37, no. 7, 1 July 1989 (1989-07-01), pages 669-676, ISSN: 0090-6778, or
D7: EYUBOGLU M V; QURESHI S U H: "REDUCED-STATE SEQUENCE ESTIMATION FOR CODED MODULATION ON INTERSYMBOL INTERFERENCE CHANNELS" IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, vol. 7, no. 6, August 1989 (1989-08), pages 989-995,

and because of lack of inventive step (Articles 52(1) EPC and 56 EPC 1973) having regard to a combination of D1 with D2 or with D7.

II. The notice of appeal was received on 14 December 2006. The appeal fee was paid on the same day. The statement setting out the grounds of appeal was received on 23 February 2007. The appellant requested that the appealed decision be set aside and that a patent be

granted on the basis of the documents on which the appealed decision was based, namely claims 1 to 7 filed by fax on 28 September 2005 and claims 8 and 9 filed with letter of 8 October 2004. Oral proceedings were requested on an auxiliary basis.

III. A summons to oral proceedings to be held on 11 November 2010 was issued on 25 August 2010. In an annex accompanying the summons the board expressed the preliminary opinion that the subject-matter of the independent claims did not fulfil the requirements of Articles 52(1), 54(2), 56 and 84 EPC. The board gave its reasons for the objections and stated that the appellant's arguments were not convincing.

IV. In response to the appellant's submissions dated 3 September 2010 the board agreed to postpone the date of the oral proceedings to 26 November 2010.

V. With a letter dated 25 October 2010 the appellant submitted four sets of claims according to a main request and first to third auxiliary requests together with arguments that these claims fulfilled the requirements of Article 84 EPC, were novel and met the requirements of Article 56 EPC.

VI. Independent claim 1 according to the main request reads as follows:

"1. A method for processing a signal received from a dispersive channel, said channel being modeled as a filter having L taps, said method comprising the steps of:

processing intersymbol interference due to more significant taps with a reduced state sequence estimation technique; and
processing intersymbol interference due to less significant taps with a cancellation algorithm using tentative decisions, wherein said cancellation algorithm is of lower complexity than said reduced-state sequence estimation technique."

Independent claim 1 according to the first auxiliary request differs from claim 1 of the main request by the following additional feature:

"and wherein said processing intersymbol interference due to less significant taps step is performed prior to said processing intersymbol interference due to more significant taps."

Independent claim 1 according to the second auxiliary request differs from claim 1 of the first auxiliary request by the following additional feature for the first processing step:

"wherein said reduced state sequence estimation technique cancels an ISI contribution from taps 1 to U"

and by the following additional feature for the second processing step:

"and cancels an ISI contribution from taps U+1 to L,".

Independent claim 1 according to the third auxiliary request reads as follows:

"1. A method for processing a signal received from a dispersive channel, said channel being modeled as a filter having L taps, said method comprising the steps of:
processing intersymbol interference due to more significant taps with a reduced state sequence estimation technique, wherein said reduced state sequence estimation technique cancels an ISI contribution from taps 1 to U based on a trellis and a decision feedback unit, wherein said trellis accounts for an ISI contribution from taps 1 to K and wherein said decision feedback unit cancels an ISI contribution from taps K+1 to U; and
processing intersymbol interference due to less significant taps with a cancellation algorithm using tentative decisions, wherein said cancellation algorithm is of lower complexity than said reduced-state sequence estimation technique and cancels an ISI contribution from taps U+1 to L, and wherein said processing intersymbol interference due to less significant taps step is performed prior to said processing intersymbol interference due to more significant taps."

Independent claims 5 of all requests are directed to a corresponding receiver.

VII. By facsimile received on 25 November 2010 the appellant informed the board that it would not be represented at the oral proceedings.

VIII. The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the main request, or, subsidiarily, on

the basis of any of the first, second or third auxiliary requests as filed with letter dated 25 October 2010.

IX. Oral proceedings were held on 26 November 2010 in the absence of the appellant. After due deliberation on the basis of the written submissions in the statement setting out the grounds of appeal, the letter of 25 October 2010 and the requests, the board announced its decision.

Reasons for the Decision

1. Admissibility

The appeal complies with the provisions of Articles 106 to 108 EPC 1973, which are applicable according to J 0010/07, point 1 (see Facts and Submissions, point II above). Therefore the appeal is admissible.

2. Non-attendance at oral proceedings

In its letter of 25 November 2010 the appellant announced that it would not be represented at the oral proceedings. The board considered it expedient to maintain the date set for oral proceedings. Nobody attended the hearing on behalf of the appellant.

Article 15(3) RPBA stipulates that the board shall not be obliged to delay any step in the proceedings, including its decision, by reason only of the absence at the oral proceedings of any party duly summoned who

may then be treated as relying only on its written case.

Thus, the board was in a position to take a decision at the end of the hearing.

Main request

3. Article 84 EPC

3.1 Independent method claim 1 specifies a sequence of steps which is not supported by the description. Claim 1 leaves open whether the step of using reduced state sequence estimation (RSSE) takes place before the step of using an algorithm of lower complexity (e.g. decision feedback equalizer DFE). This is in contrast to original claim 1 and to column 3, lines 5 to 8, ("The DFE technique initially removes the intersymbol interference associated with the tail taps, then the RSSE technique is applied only to the more important tail taps" - emphasis added) and column 4, line 41 ("Thereafter") or line 44 ("initially") of the application as published. Claim 1 is therefore not supported by the description in this regard.

3.2 In addition, the expression "lower complexity" was objected to in the appealed decision. The appellant argued that the complexity of an algorithm according to claim 1 was based on the number of taps. However, as is apparent from the examining division's argument that the complexity can depend on the number of computations required to carry out the algorithm, the board is not convinced by the appellant's argument that the skilled person would recognise that the claimed invention is

directed to the number of taps as the criterion for complexity. In the light of the fact that the application explicitly refers to the hardware complexity (see the last sentence of paragraph [0016] of the published application), it is conceivable that the complexity depends on the space for a hardware implementation on a chip and it is at least unclear according to which criterion it is to be decided whether the complexity is "lower", rendering the wording of claim 1 unclear. The appellant's arguments submitted with letter dated 25 October 2010 (see page 2, last paragraph onwards), based on the assumption of a decision feedback unit DFU with parallel decision feedback cells DFC, are not convincing, because the wording of a claim has to be clear in itself without there being a need for the skilled person to refer to the description (see e.g. T 1129/97, OJ EPO 2001, 273). Claim 1, however, in contrast to the specific embodiment of the description referred to by the appellant, does not specify a decision feedback unit DFU with parallel decision feedback cells DFC and therefore does not allow the skilled person to infer according to which criterion it is to be decided whether the complexity is "lower".

Claim 1 therefore does not to fulfil the requirements of Article 84 EPC.

First auxiliary request

4. Article 84 EPC

4.1 In the appealed decision, independent claim 1 was objected to because the expressions "more significant

taps" and "less significant taps" were considered to be unclear. The board agrees that there is no established meaning of these expressions in the art.

4.2 According to the appellant's argumentation, an interpretation of the expressions objected to in the light of the description could be based either on the tap value or the tap position. With regard to an interpretation directed to the tap value, the appellant referred to the following passage of the description: "the initial taps provide the largest contribution to the signal energy of the channel output, and the corresponding power decreases to zero as the taps approach infinity" (see paragraph [0012] of the application as published). However, for referring to a tap value, as argued by the appellant, it remains unclear what exactly is such a "largest" contribution (e.g. 60% or 80% etc.). The disclosure is silent in this regard, leaving the skilled reader in doubt as to how to distinguish between more significant and less significant taps.

4.3 Regarding an interpretation directed to the tap position, the description discloses that "the less significant tail taps (U+1 through L) are processed with a lower complexity cancellation algorithm, such as a decision-feedback equalizer (DFE) technique, that cancels the tail taps using tentative decisions. Thereafter, only the more significant initial taps (1 through U) are processed with a reduced state sequence estimation (RSSE) technique." (see paragraph [0008] of the application as published).

4.4 The application fails to give any embodiment for a concrete value of U. According to e.g. column 3, line 15, "a well-chosen value of U" is required. According to the last sentence of paragraph [0016] of the published application, the "design parameter U" is a crucial feature for solving the problem of the invention, which, however, is not specified in claim 1. While the board agrees with the appellant's argument that the "predefined percentage of the overall signal energy" is a design choice (see page 2, second paragraph of the letter dated 25 October 2010), claim 1 neither makes reference to the "overall signal energy" nor gives any information regarding the position U being the criterion on which a distinction between more significant taps and less significant taps is to be made.

Therefore, the subject-matter of claim 1 is considered to be an undue generalisation of the "overall signal energy". Claim 1 is therefore not supported by the description in the whole range claimed.

Claim 1 therefore does not fulfil the requirements of Article 84 EPC.

4.5 The expression "lower complexity" is still part of claim 1 and the afore-mentioned problem of lack of clarity therefore persists.

Claim 1 therefore does not fulfil the requirements of Article 84 EPC, for the reasons set out in point 3.2.

Second auxiliary request

5. Article 84 EPC

The expression "lower complexity" is still part of claim 1 and the problem of lack of clarity as presented above therefore persists.

Claim 1 therefore does not fulfil the requirements of Article 84 EPC, for the reasons set out in point 3.2.

Third auxiliary request

6. Article 123(2) EPC

The board has doubts that the application provides for a direct and unambiguous disclosure of the parameter K introduced with the added features of this request, in particular with regard to the relation between the parameters U and K. Paragraph [0015] of the published application refers to an Index "k" for the channel taps f_k, followed by a relation $K \leq U \leq L$ for "K" (i.e. capital K). In the next paragraph it is disclosed that K can be the number of taps that are accounted for in the combined code and channel state inside the RSSE circuitry 500. The exact relation between K and U according to the added feature of claim 1 of this request is, however, ambiguous.

7. Article 84 EPC

The expression "lower complexity" is equally part of claim 1. For the reasons given above (see point 3.2),

claim 1 does not fulfil the requirements of Article 84 EPC.

8. Inventive step - Article 56 EPC

Even if the requirements under Articles 84 and 123(2) EPC were fulfilled, the subject-matter of claim 1 of this request at least would not involve an inventive step.

8.1 D1, which is considered to be the closest prior art document, discloses a decision feedback equalizer DFE as a prefilter to a Viterbi Decoder VA, in which the DFE has been embedded to truncate the channel impulse response through feedback subtraction (see figure 2, section II of D1), which is suitable for processing a signal received from a dispersive channel (see e.g. page 971, right-hand column, second paragraph) and which is modelled as a filter having taps (see in particular equations 2 and 3). In the board's view figure 2 of D1 can be compared to figures 2 and 4 of the published application with the exception that figure 2 of D1 shows a Viterbi algorithm VA in contrast to element 500 in figure 2 of the application showing the reduced state sequence estimation (RSSE) circuitry.

8.2 In the decision under appeal it was argued that the feature of a reduced state sequence estimation (RSSE) algorithm of claim 1 could be interpreted in a broad manner. The examining division argued that from the disclosure "the first V out of the total number of v of intersymbol interference terms are to be operated on by the VA ..., resulting in an M^V-state receiver" (see the text following equation 2 of D1) it followed that a

reduced state sequence estimation (RSSE) was used, since V was smaller than v and the number of trellis states was reduced from M^v to M^V. D1 further disclosed that the remaining intersymbol interference should be equalised with DFE making a tentative decision (which corresponds to the embodiment given in paragraphs [0008] and [0013] of the description of the published application).

8.3 The board agrees with the examining division that the formulation of the feature "a reduced state sequence estimation technique" of claim 1 can be interpreted in a broad manner, since the application does not give a concrete definition of what exactly is to be understood by this expression according to the claimed invention, hence not limiting the scope of this feature. Therefore any technique which cancels intersymbol interference (ISI) contribution taps and which can be regarded as RSSE falls under the scope of claim 1. In principle, the reduced-state sequence estimation is a detection algorithm that provides a direct trade-off between complexity and performance in the presence of intersymbol interference channels by reusing determined data in order to reduce the hardware size (as also disclosed in D1, e.g. page 973, left-hand column, last sentence of second paragraph, or section IV). It employs the basic idea of set partitioning for obtaining reduced state trellises (see for example paragraphs [0005] and [0006] of the published application).

8.4 In the passage "the first V out of the total number of v of intersymbol interference terms are to be operated on by the VA ..., resulting in an M^V-state receiver"

(see page 972, right-hand column, last paragraph), D1 explicitly discloses that this is done with the "first" intersymbol interference (ISI) terms. According to claim 1 the more significant taps are usually the intial taps or taps 1 to U. By operating with a Viterbi algorithm on the first V of the ISI terms, D1 discloses processing the more significant taps with the reduced state decoder. The "rest" of the ISI terms are equalised by a DFE as a prefilter (see figure 2 of D1), which terms can apparently therefore be regarded as the less significant taps being processed prior to the ISI due to the more significant taps according to claim 1.

8.5 Since DFE is used for equalisation, the board does not agree with the appellant's argument that D1 used the DFE only to reduce the number of states and taught away from the use of DFE to reduce the number of taps (see the paragraph bridging pages 4 and 5 of the statement setting out the grounds of appeal). The subject-matter of claim 1 requires that all L taps are processed either with RSSE or with a cancellation algorithm using tentative decisions such as DFE.

8.6 According to the description of the application as referred to above, under certain circumstances (here DFSE being a specialisation of RSSE for U=K becomes a pure Viterbi decoder) RSSE can result in using a Viterbi algorithm for processing intersymbol interference. The appellant argued that the claims did not cover the case of a DFSE with U=K (see the statement setting out the grounds of appeal, page 3, paragraphs 4 and 5). In particular, the statement "The limitations in the cited claim … do not contradict the statements in the specification that … the present

invention includes the case U equal to K" is not clear to the board. Because of the appellant's absence during oral proceedings, this issue could not be clarified. The board still has doubts that this is correct, because the corresponding feature of claim 1 does not exclude the embodiment with U=K as described in the application.

8.7 Even if one assumed that the special case with U=K as disclosed in the present application was not comprised by the subject-matter of claim 1, and one interpreted the feature of a reduced state sequence estimation (RSSE) algorithm in a narrow manner (having a particular meaning as argued by the examining division), it has to be considered that D1 already suggests the idea of reducing the number of intersymbol interference (ISI) terms to be operated on by the Viterbi algorithm (see page 972, equation (2) and subsequent text). D1 explicitly suggests to "simplify the VA itself" (see page 972, left-hand column, fourth paragraph).

The skilled reader of D1 is therefore motivated to take other reduced state techniques into consideration in order to find a solution for the problem of reducing hardware complexity and optimising the critical path of the Viterbi algorithm used in D1, which is considered to be the objective problem underlying the only difference between the subject-matter of claim 1 and the teaching of D1, i.e. the concrete type of algorithm used for reducing the number of trellis states.

8.8 As described in the introductory portion of the present application, RSSE was a technique which was well known before the priority date of the present application. As

an example, see the publication D2 which discloses a reduced-state decoding technique similar to the embodiment using DFSE described in paragraph [0024] of the present application (see D2, page 671, left-hand column onwards, in particular the disclosure dealing with the case K<L). D2 even makes reference to a MLSD receiver as used in D1 and is therefore compatible with the teaching of the closest prior art. Since DFSE is a specialisation of RSSE which is encompassed by the subject-matter of claim 1, D2 discloses RSSE according to the invention for the ISI terms 0 to K. The remaining L minus K ISI terms are compensated in a decision-feedback fashion which implies the use of a DFE technique according to the added feature of claim 1 of this request, i.e. a trellis accounts for an ISI contribution from taps 1 to K and a decision feedback unit cancels an ISI contribution from taps K+1 to the last tail tap.

8.9 This is in contrast to the appellant's argument that D2 computed all of the ISI terms using an RSSE technique (see page 4, paragraph 4 of the statement setting out the grounds of appeal), which therefore does not convince. The board interprets D2 to the effect that the ISI terms 0 to K can be considered to correspond to the more significant taps, whereas the remaining K to L ISI terms correspond to the less significant taps. Hence, D2 discloses a reduced-state decoding technique similar to the DFSE of the embodiment described in paragraph [0024] of the present application (see D2, page 671, left-hand column onwards) and further implies the use of DFE for processing ISI terms. D1 discloses placing a DFE in front of the Viterbi decoder. As argued above, the board does not agree with the

appellant's argument that D1 used the DFE only to reduce the number of states and taught away from the use of DFE to reduce the number of taps. The subject-matter of claim 1 requires that taps 1 to U are processed with a reduced-state sequence estimation algorithm RSSE and taps U+1 to L are processed with a cancellation algorithm using tentative decisions such as DFE. The board therefore judges that the skilled person would take a combination of the teaching of D1 with that of D2 into consideration without the use of inventive skills, thereby arriving at a solution of the objective problem by using the RSSE technique DFSE instead of the Viterbi decoder disclosed in D1.

8.10 As far as the appellant's argument on page 4, paragraph 4 of the statement setting out the grounds of appeal and on page 8, paragraph 3 of the letter dated 25 October 2010 regarding the allegedly surprising results of the claimed invention is concerned, the board notes that even if the publications mentioned by the appellant contained such a statement, this is merely a secondary consideration showing the subjective opinion of the authors, but not an objective reasoning that an inventive activity was involved. It has to be considered that the author of the publications referred to by the appellant is one of the inventors of the present application. The statements in the cited publications therefore only show that the inventor has overcome his own prejudice which is not considered to be an indication of the existence of an inventive step. In particular, no indication is given that there had been an objective long-felt need for a solution or an objective technical prejudice in the art which could indicate that technical hurdles had to be overcome.

This argument of the appellant is therefore not convincing.

Therefore the board concludes that the subject-matter of claim 1 is obvious in the light of a combination of the teachings of publications D1 and D2.

9. Thus, none of the four requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Götz A. Ritzka