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Datasheet for the decision of 11 October 2010

Case Number: T 0793/07 - 3.5.02

Application Number: 01105577.9

Publication Number: 1139565

IPC: H03K 5/13

Language of the proceedings: EN

Title of invention:
Synchronous delay circuit

Applicant:
Renesas Electronics Corporation

Headword:
-

Relevant legal provisions:
EPC Art. 83

Relevant legal provisions (EPC 1973):
-

Keyword:
"Sufficiency of disclosure (no) - all requests"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0793/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 11 October 2010

Appellant: Renesas Electronics Corporation
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 21 December 2006 refusing European patent application No. 01105577.9 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: R. Lord
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal of the applicant against the decision of the examining division to refuse European patent application No. 01 105 577.9.

II. The reason given for the refusal was that the application did not meet the requirements of Article 83 EPC.

III. Of the documents cited during the procedure before the first instance, the following is relevant for this decision:

D3: EP 0 907 251 A.

Oral proceedings before the board took place on 11 October 2010. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claim 1 filed with a letter dated 4 October 2004 and claims 2 to 11 filed with a letter dated 2 July 2002, subsidiarily on the basis of claim 1 of the first or the second auxiliary request filed with a letter dated 27 September 2010, and claims 2 to 11 filed with letter dated 2 July 2002.

IV. Claim 1 according to the appellant's main request reads as follows:

"A synchronous delay circuit apparatus comprising:

a plurality of sets of synchronous delay circuits (100, 101), each set including a first delay circuit chain (11, 13) for delay measurement, along which input clock signals (3) propagate, and a second delay circuit

chain (12, 14) connected to said first delay circuit chain, a difference being measured by said first delay circuit chain (11, 13), the difference being measured between the delay time of a preset circuit or path for propagating and outputting clocks and the period of input clocks, said second delay circuit (12, 14) chain reproducing and outputting the measured time difference;

wherein at least one (101) of said sets of synchronous delay circuits (100, 101), in combination with at least one delay circuit (6), has a measured delay quantity different from that of the other or others of the synchronous delay circuits, without causing discontinuity in clocks output from said synchronous delay circuits to said preset circuit or path even when the relative relation in the magnitudes between the delay time of the preset circuit (4) or path and the period of said input clock is changed."

Claim 1 according to the appellant's first auxiliary request reads as follows:

"A synchronous delay circuit apparatus comprising:

(a) a plurality of sets of synchronous delay circuits (100, 101), each set including a first delay circuit chain (11, 13) for delay measurement, along which input clock signals propagate, and a second delay circuit chain (12, 14) using said first delay circuit chain the difference being measured between the delay time of a preset circuit or path for propagating and outputting clocks and the period of input clocks, said second delay circuit chain reproducing and outputting the measured time difference;

(b) wherein at least one (101) of said sets of the synchronous delay circuits (100, 101) being added with

at least one delay circuit (6), has a measured delay quantity different from that of the other or others of the synchronous delay circuits, at least one of outputs (E, F) of said plurality of sets of synchronous delay circuits (100, 101) being always supplied to said preset circuits or path as an input signal of a switching over unit (10) for switching over between said at least one of the outputs (E, F) and the input clocks (3), thereby causing no discontinuity in clocks output from said synchronous delay circuits to said preset circuit or path even when the relative relation in the magnitudes between the delay time of the present [sic] circuit (4) or path and the period of said input clock is changed."

Claim 1 according to the appellant's second auxiliary request differs from that according to his first auxiliary request in that the words "having a means" are inserted after the expression "switching over unit (10)" in paragraph (b), in that the word "causing" in the same paragraph is misspelt "causig", and in that the following text is added at the end of the claim:

"; and

(c) wherein in one set of said plurality of sets of synchronous delay circuits (100, 101), time difference of a varied delay time of said preset circuit or path caused by delaying one of output and input of said preset circuit or path from the period of said input clock signals is measured by said first delay circuit chain (11, 13), and thus measured time difference is reproduced by said second delay circuit chain (12, 14) for output."

V. The appellant essentially argued as follows:

The skilled person reading the application would have recognised that the combination of the two internal clock signals could not be by switching over between them, so that paragraph [0036] and claim 5 of the published application were clearly wrong, and would further have realised that the two internal clock signals were identical except for the dropped clock pulse in one of them, as a result of which it would have been immediately apparent to him that the combination of these two signals to produce a clock signal free of errors should be in the form of an "OR"-combination. Such a combination was taught by the passages at column 11, lines 30 to 37 and column 12, lines 51 to 57 of the published application.

It was clear from the application documents that the starting point for the invention was the prior art apparatus described with reference to Figs. 5 to 9, with the functionality of the switching over unit being essentially as described in D3, so that no switching over between the two internal clock signals was required.

It was also clear from the application documents that the synchronism between the two internal clock signals, which was a prerequisite for the functioning of the "OR"-combination, was provided by the arrangements in both of Figs. 1 and 4. In particular, the circuit of Fig. 4 did not require the additional delay circuit 8 because, compared to the circuit of Fig. 1, the delay circuit 6 was positioned at the other input of the delay detection circuit 7.

The board had not correctly applied the case law relating to the capabilities of the person skilled in the art, specifically that these should be the same for the assessment of sufficiency of disclosure and inventive step, in which respect he referred to what he described as an "Example claim", which he argued demonstrated this divergence. In particular, the skilled person was, according to section II.A.2 a) of the published "Case Law of the Boards of Appeal of the European Patent Office", able to correct errors and fill in gaps in the teaching of the application.

Claims corresponding to those of his main request had been granted by the patent offices of the USA, Japan, Korea, China and Taiwan, with no objections relating to sufficiency of disclosure having been raised.

Reasons for the Decision

1. The appeal is admissible.

Sufficiency of disclosure (Article 83 EPC)

2. The invention described in the present application and defined in the independent claims according to each of the appellant's requests aims to solve the technical problem in the prior art clock synchronisation circuit described in the application with reference to Figs. 5 to 9 that jitter in the external clock signal can lead to clock pulses being dropped in the output clock signal.

2.1 From the description of the application it is immediately apparent that the solution to this problem requires not only the provision of the second synchronous delay circuit (circuit 101 in Figs. 1 and 4) with the additional delay element(s) (delay circuit 6 in Figs. 1 and 4 and delay circuit 8 in Fig. 1), but also the provision of additional functionality in the "switching over unit" (10 in Figs. 1 and 4), which, compared to that in the prior art, is required to not only select between the external clock signal and that generated by the synchronous delay circuits, but also, following synchronisation, to generate the clock signal to be applied to the clock tree from the outputs of the two synchronous delay circuits in such a manner that a continuous clock signal is provided to the clock tree.

2.2 The application describes explicitly in paragraph [0036] of the published application and dependent claim 5 (which in all of the appellant's requests remains in its original form) that the "switching over unit" carries out exactly the function which its name implies, i.e. it switches so as to direct a selected one of the three clock signals (the two internal clock signals generated by the synchronous delay circuits and the external clock signal) to the input of the clock tree. However, the application provides no teaching as to how this switching should be carried out, in particular what criteria should be used to decide which of the two internal clock signals should be selected. Given that both the external clock period and the delay period of the clock tree would be subject to fluctuations, the implementation of this aspect of the switching over unit would not be straightforward. Since the various passages of the description which mention the

functioning of the switching over unit only describe the general object to be achieved by the switching over unit, and not how it achieves that object, these cannot provide the skilled person with any information in that respect. Thus the disclosure of the application is not sufficient to enable the skilled person to implement the switching over unit.

2.3 On this basis the board concludes that the application does not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art, thus not satisfying the requirements of Article 83 EPC.

3. The appellant argued that the skilled person considering the technical problem posed in the present application would immediately recognise that in order to generate an uninterrupted clock signal from the two internal clock signals switching was not only impossible but also unnecessary, because the required signal could be simply generated by carrying out an "OR"-combination of the two internal clock signals. In particular he argued that the passages at column 11, lines 30 to 37 and column 12, lines 51 to 57 of the published application disclosed that the "switching over" function was a switching between, on the one hand, the external clock signal, and on the other hand the combination of the two internal clock signals. On the basis of these two points he also argued that the skilled person would have concluded that the statements in paragraph [0036] and claim 5 of the application were erroneous, so should be ignored. He concluded that the actual switching function (in contrast to the "OR"-combination) was the same as that already disclosed in

detail in D3, which was clearly the starting point for the invention.

3.1 The board is not convinced by the above argumentation concerning the disclosure in the two passages cited in columns 11 and 12, because the wording used there is ambiguous, and could be understood to mean either the switching between two alternatives (external clock or combined internal clocks) described by the appellant, or switching between all three input signals, as argued in paragraphs 2.1 and 2.2 above. Given this ambiguity in the application, the skilled person would be expected to initially look elsewhere in the application itself to clarify these passages, and would thus recognise that paragraph [0036] and claim 5 of the application provide an unambiguous clarification of this point, namely that the switching over function includes switching between the two internal clock signals. The board notes also that this interpretation of the description and claims is confirmed by the symbol used in the figures of the application to represent the switching over unit, namely the symbol for a multiplexer, which implies the function of selection between the inputs.

3.2 The board is also not convinced by the appellant's argument that the skilled person would consider that switching between the two internal clock signals would be impossible, so that he would immediately consider alternatives. The board acknowledges that the skilled person would recognise that this switching would be problematic, this being an inherent part of the argumentation in paragraphs 2.1 and 2.2 above. However the board considers that the skilled person would not

go so far as to conclude from this that the switching between the internal clocks would be impossible. On the contrary, it appears to the board to be entirely plausible that the skilled person would conclude from the application documents that such switching was possible, but relied on a technique of which he was not aware. Thus he would not conclude from the application that the invention was not intended to make use of switching, but was instead intended to make use of some other form of routing of the internal clocks to the clock tree. Given this conclusion, the question as to whether the skilled person would then realise that this other form of routing would involve an "OR"-combination does not arise. For this reason also the appellant's argument based on his "Example Claim" is not relevant to this decision.

3.3 In support of the argument discussed in the previous paragraph, the appellant also argued that the application clearly teaches that the invention starts from the prior art described with reference to Figs. 5 to 9, so that it was also clear that the switching unit should have the same functionality as described there, and described in more detail in D3, so that no switching between the two internal clock signals was required.

3.3.1 The board does not find this argument convincing for two reasons. Firstly, the application does not clearly and unambiguously teach that the invention is to be seen as a direct development from the circuit of Figs. 5 to 9. Secondly, even if that were the case, the fact that the invention might start from a circuit in which the switching over unit has the limited functionality

described in D3, when there is only one internal clock signal, would not allow the skilled person to draw any clear conclusions as to whether that would still be the case for the circuit of the invention, in which there are two internal clock signals, i.e. as to whether the switching functionality should be extended to include the additional clock signal, or whether an alternative function, such as an "OR"-combination should be introduced to cope with the additional signal.

3.3.2 In the context of this last point, the board observes also that the application documents provide no further hints or suggestions that an "OR"-combination should be used to process the two internal clock signals. In particular the question arises as to whether or not the circuit provides the synchronism between these two clock signals which would be necessary for such an "OR"-combination to function properly. In this respect, the application provides no explicit teaching, even though the skilled person would probably be able to derive the teaching that such synchronism would be achieved from the description of the overall functioning of the circuit. Of most relevance to this question is the arrangement of the delay circuits 6 and 8 in Figs. 1 and 4, but the description of these elements provides no suggestion that they are linked to this requirement.

3.4 The appellant has argued that the above reasoning, particularly that in paragraphs 3.1 and 3.2, is not consistent with the case law of the boards of appeal with respect to the abilities of the person skilled in the art, in which context he referred to section II.A.2 a) of the published "Case Law of the Boards of Appeal

of the European Patent Office", which states also that these abilities should be the same whether considering sufficiency of disclosure or inventive step. Specifically, he argued that according to that case law, the skilled person was able to fill in missing teaching and correct errors in the application. The board does not find this argument convincing, because in order for the skilled person to deduce from the application that the switching over unit should use an "OR"-combination of the two internal clock signals, he would have to initially recognise that the disclosure of paragraph [0036] and claim 5 was erroneous, which the board considers would not be obvious to him (see paragraph 3.2 above). Thus the question as to whether, having recognised such an error, the skilled person would then be able to correct the error and fill in the missing teaching does not arise.

3.5 Finally the appellant argued that it was relevant to the present case that five other patent offices have granted patents for the invention of the present application without raising objections concerning sufficiency of disclosure. Besides the obvious point that the granting of a patent in other jurisdictions provides no clear indication as to whether the requirements of the EPC are satisfied, the board notes also that in four of the cited jurisdictions (Japan, Korea, China and Taiwan) the language of the application was different, so that it cannot be excluded that the absence of an objection arose from the different terminology used in those applications.

4. The above arguments relate to the disclosure of the original application and the nature of the invention as

originally disclosed. The different forms of wording used to define that invention in the independent claims of the appellant's three requests has no impact on those arguments. The conclusion of paragraph 2.3 above therefore applies to all three requests. Hence none of the appellant's requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu