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Datasheet for the decision of 24 January 2013

Case Number: T 0698/08 - 3.4.03

Application Number: 01931109.1

Publication Number: 1261987

IPC: H01L 21/28, H01L 21/8247, H01L 29/788, H01L 27/115

Language of the proceedings: EN

Title of invention:
Single tunnel gate oxidation process for fabricating NAND flash memory

Applicant:
Spansion LLC

Opponent:
-

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
T 0184/82

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0698/08 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 24 January 2013

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 28 November 2007 refusing European patent application No. 01931109.1 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: V. L. P. Frank
T. Karamanli

Summary of Facts and Submissions

I. This is an appeal against the refusal of European patent application No. 01 931 109 for the reason of lack of inventive step.

II. As final requests on appeal the applicant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the claims according to the main request, or the 1st or 2nd auxiliary request, all submitted with letter of 19 December 2012.

Auxiliarily oral proceedings were requested.

III. Claim 1 of the main and the 1st auxiliary request reads as follows:

1. "A method of fabricating NAND flash memory, the method comprising:
forming a first region of first conductivity type (22) over a semiconductor substrate (20);
then forming a first oxide layer (24) over said first region of first conductivity type in a select gate area and a memory cell area; and
characterised by then forming a second region of second conductivity type (62) in the first region, at least partially below an opening in the first oxide layer, the second region shared by the select gate area and the memory cell area; wherein the thickness of the first oxide layer in the select gate area is substantially the same as the thickness of the first oxide layer in the memory cell area."

Claim 10 of the 2nd auxiliary request differs from claim 1 of the main request in that in the feature:

"then forming a first oxide layer (24) over said first region of first conductivity type in a select gate area and a memory cell area"

the expression "then" was omitted; and in that the following feature was appended:

"the memory cell comprising a fourth region (21) of second conductivity type enclosing the first region of a first conductivity type."

IV. The following document is mentioned in this decision:

D1 = US 5 877 980 A

V. The examining division found that:

- The method of claim 1 of the main request differed from the method disclosed in document D1 only in that the second region of second conductivity type in the first region was formed at least partially below an opening in the first oxide layer, thus separating the select gate oxide layer and the memory cell oxide layer from each other. The application however did not disclose why these oxide layers should be separated and which technical problem was solved by such process step. The doping of the third semiconductor region was performed by ion implantation in the present application as well as in D1. This could be done with or without a gate

oxide layer being present. The skilled person therefore would have removed or not the gate oxide prior to implantation according to the circumstances.

VI. The appellant applicant argued in writing essentially as follows:

- The present claims included the limitation that the select gate oxide layer and the memory cell oxide layer were separated from each other above a portion of the third region of second conductivity type forming the source/drain region. This separation was not present in the prior art and conferred a technical advantage over the devices of the prior art. In presence of the oxide layer, the step of doping the source/drain region resulted in some dopant present in the oxide layer, such dopants extending beyond the source/drain region and providing a mechanism for shorting the floating gate and the source/drain. With the oxide layer removed, or substantially removed, the danger of shorting was significantly reduced. There was no suggestion in Dl of such removal of the oxide layer, and that such removal reduced the risk of shorting the floating gate and the source/drain.

- Furthermore, D1 did not disclose an opening in the first oxide layer. D1 only showed in each of its figures a uniform and intact gate oxide film. Dl required an intact gate oxide film, since the method of Dl disclosed the steps of forming the source/drain regions, first insulating film and PA-plate as follows: impurities were implanted on the sides of the wordlines into a portion of the

semiconductor substrate, thereby forming the source/drain regions, then the first insulating film was formed, then conductive material was deposited on the resultant structure and the conductive film was patterned to form the PA-plate. Thus, in D1, the gate oxide film had to be intact over the source/drain regions so as to protect the semiconductor substrate and the source/drain regions from at least the deposition of the first insulating film.

VII. In a communication pursuant to Article 15(1) RPBA annexed to the summons to oral proceedings, the board informed the appellant of its provisional opinion that the subject-matter of the independent claims of the then sole request did not involve an inventive step for the reasons given in the decision under appeal.

VIII. The appellant's representative announced with letter dated 17 January 2013 that he would not attend the oral proceedings.

IX. Oral proceedings were held on 24 January 2013 in the absence of the applicant.

Reasons for the Decision

1. The appeal is admissible.

2. As announced in advance, the duly summoned appellant did not attend the oral proceedings. According to Rule 71(2) EPC 1973, the proceedings could however continue without him. In accordance with Article 15(3) RPBA, the

board relied for its decision only on the appellant's written submissions. The board was in a position to decide at the conclusion of the oral proceedings, since the case was ready for decision (Article 15(5) and (6) RPBA), and the voluntary absence of the appellant was not a reason for delaying a decision (Article 15(3) RPBA).

3. *Main request - Inventive step (Article 56 EPC 1973).*

3.1 It is undisputed that document D1 discloses in the words of claim 1 (column 1, lines 5 to 15; column 8, line 66 to column 10, line 60; Figures 10 to 12):

A method of fabricating NAND flash memory, the method comprising:
forming a first region of first conductivity type (P-type region 201) over a semiconductor substrate (101);
then forming a first oxide layer (the select gate oxide layer and the memory cell oxide layer 350) over said first region of first conductivity type in a select gate area and a memory cell area; and
then forming a second region of second conductivity type (source/drain region 370) in the first region, the second region shared by the select gate area and the memory cell area; wherein
the thickness of the first oxide layer in the select gate area is substantially the same as the thickness of the first oxide layer in the memory cell area (the thickness of the oxide layer 350 is constant along the whole NAND wordline, see figures 10B to 12B).

3.2 The method of claim 1 differs from the method disclosed in document D1 in that the second region (ie the source/drain region) is formed "at least partially below an opening in the first oxide layer" (ie the source/drain region is formed beneath the opening separating the select gate oxide layer and the memory cell oxide layer). In the following this feature will be referred to as the "distinguishing feature".

3.3 The application discloses that the technical problem addressed by the invention is to provide a single tunnel gate oxidation process for fabricating NAND memory strings where the gate oxide of the select transistors and that of the floating gate memory transistors are fabricated in a single oxidation step, so that the select gate transistors and the floating gate memory transistors have the same oxide thickness (page 1, line 37 to page 2, line 1).

3.4 According to the problem-solution approach applied by the boards, the objective technical problem may differ from the one originally stated in the application, in particular when more relevant prior art is available. This may lead to a reformulation of the technical problem addressed by the invention. The reformulated "objective" technical problem may be based on any technical effect provided by the invention as long as that effect is derivable from the application as filed. In T 184/82 (OJ EPO 1984, 261) the board stated that "regarding the effect of the invention" reformulation of the problem could be allowed "provided the skilled man could recognize the same as implied or related to the problem initially suggested". The problem may also be restated to a less ambitious objective, ie providing

an alternative to the known solution, but the skilled person should be able to deduce it from the original disclosure when considered in the light of the closest prior art (see Case Law of the Boards of Appeal, 6th ed. 2010, I.D.4.4).

3.5 The select gate transistors and the floating gate memory transistors of the NAND structure disclosed in document D1 are formed in the same oxidation process and have the same oxide thickness (D1, column 9, lines 30 to 35; Figure 10B). Furthermore, the "distinguishing feature" is not related to the technical problem mentioned in the application, since it concerns the formation of the source/drain region and not the formation or the thickness of the oxide layer. Hence the technical problem addressed by the invention has to be reformulated having regard to document D1.

3.6 The appellant applicant argued that the "distinguishing feature" (ie the removal of the oxide layer above the source/drain regions prior to ion implantation) had the effect that it significantly reduced the danger of shorting between the floating gate of the memory cell and the source/drain region, since doping the source/drain region by ion implantation in the presence of the oxide layer resulted in some dopant present in the oxide layer, increasing its conductivity.

The appellant further argued that the skilled person would not consider removing the oxide layer above the source/drain regions, since it reduced the protection of the semiconductor substrate achieved by an intact oxide layer from the further device processing steps, eg the deposition of the first insulating film.

3.7 The application discloses in relation to the "distinguishing feature" that *"Fig. 6 depicts the structure of FIG. 5 after* ***a section 60 of oxide layer 24****, first polysilicon layer 30, separation layer 40, and second polysilicon layer 50* ***has been etched away****, exposing P-well 22. A medium doped source/drain region shared by select transistor 12 and core memory cell 13 is then implanted"* (page 3, lines 12 to 25; figures 6 and 11; emphasis added by the board).

3.8 The board considers that the skilled person would not derive from this scarce disclosure that the removal of the oxide layer prior to the formation of the source/drain region is related to the possibility of shorting the floating gate. Furthermore, document D1 is silent about any drawbacks associated with the presence of the oxide layer during the ion implantation step. Hence the technical effect alleged by the appellant applicant is not derivable from the original disclosure or from the closest prior art document.

Moreover, the prejudice of removing the oxide layer adduced by the appellant, ie the reduction of protection of the semiconductor substrate, can also not be derived form the original disclosure or the closest prior art, since document D1 does not disclose any need of protecting the substrate nor the present invention discloses why this is not necessary.

3.9 Hence the board comes to the same conclusion as the examining division, namely that the skilled person had these alternatives at his disposition, ie removing or

not the oxide layer prior to ion implantation, and would choose one according to the circumstances.

3.10 The board judges, for these reasons, that the method of fabricating a NAND flash memory of claim 1 of the main request does not involve an inventive step within the meaning of Article 56 EPC 1973.

The main request is thus not allowable.

4. *1st Auxiliary request*

4.1 Claim 1 of the 1st auxiliary request is identical to claim 1 of the main request. The board judges, for the same reasons as for claim 1 of the main request, that the method of fabricating a NAND flash memory of claim 1 of the 1st auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973.

The 1st auxiliary request is thus not allowable.

5. *2nd Auxiliary request*

5.1 Claim 10 of the 2nd auxiliary request appends to claim 1 of the main request the feature:

"the memory cell comprising a fourth region (21) of second conductivity type enclosing the first region of a first conductivity type"

5.2 Document D1 however discloses that n-type region 107 is formed on the semiconductor substrate 101 and encloses P-type region 201 (D1, Figure 12B). Region 107 of D1

corresponds thus to the fourth region 21 specified in claim 10.

5.3 Hence the method of forming a NAND flash memory of claim 10 differs from the method of D1 only by the same "distinguishing feature" as claim 1 of the main request.

5.4 The board judges, for the same reasons as for claim 1 of the main request, that the method of fabricating a NAND flash memory of claim 10 of the 2nd auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973.

The 2nd auxiliary request is thus not allowable.

6. Hence none of the appellant's requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar: Chair:

S. Sánchez Chiquero G. Eliasson