

Internal distribution code:

- (A) Publication in OJ
(B) To Chairmen and Members
(C) To Chairmen
(D) No distribution

**Datasheet for the decision
of 24 August 2012**

Case Number: T 1418/08 - 3.5.06

Application Number: 04255663.9

Publication Number: 1517217

IPC: G06F 1/04

Language of the proceedings: EN

Title of invention:

Interface circuit and a clock output method therefor

Applicant:

SANYO ELECTRIC CO., LTD.

Opponent:

-

Headword:

Clock output circuit/SANYO

Relevant legal provisions:

EPC Art. 123(2)

Relevant legal provisions (EPC 1973):

EPC Art. 84, 56

Keyword:

"Original disclosure (yes)"

"Clarity (no)"

"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 1418/08 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 24 August 2012

Appellant:
(Applicant)

SANYO ELECTRIC CO., LTD.
2-5-5, Keihan-hondori
Moriguchi-shi
Osaka (JP)

Representative:

Charlton, Peter John
Elkington and Fife LLP
Prospect House
8 Pembroke Road
Sevenoaks
Kent TN13 1XR (GB)

Decision under appeal:

Decision of the Examining Division of the
European Patent Office posted 7 January 2008
refusing European patent application
No. 04255663.9 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: D. H. Rees
Members: S. Krischer
W. Sekretaruk

Summary of Facts and Submissions

I. The appeal is directed against the decision of the examining division, posted on 7 January 2008, to refuse the application 04255663.

The reason for the refusal was lack of inventive step. The following documents were used:

D1 EP 1 014 333 A1, 28 June 2000.

D2 EP 0 793 181 A1, 3 September 1997.

D3 EP 0 589 499 A1, 30 March 1994.

II. A notice of appeal was received on 14 March 2008. The fee was received the same day. A statement of the grounds of appeal was received on 13 May 2008. A main and two auxiliary requests were filed. Oral proceedings were requested.

III. The board issued a summons to oral proceedings, raising clarity objections. Inventiveness was considered to be present. It was indicated that in the light of the clarity objections, the first auxiliary request seemed to be the most promising basis for further amendments to lead to an allowable claim set. It was also noted that the description was not in order for grant.

IV. In a letter dated 6 July 2012, the appellant filed an amended first auxiliary request containing clarifications, as well as amendments to the description. A wish to avoid oral proceedings was expressed.

V. In a communication dated 13 July 2012 and sent in advance by fax on 11 July 2012, the board pointed out that oral proceedings would have to take place as long

as the appellant maintained the main request, against which the board had raised clarity objections in the summons. It noted further one minor clarity objection to the amended first auxiliary request.

VI. In a letter dated 12 July 2012, the appellant withdrew its main request. The amended first auxiliary request became the main request. The appellant further asked "whether it might still be possible to cancel the hearing".

VII. Oral proceedings were cancelled.

VIII. The appellant requests to set the decision aside and to grant a patent on the basis of a main request (claims 1-4) filed as amended first auxiliary request with letter dated 6 July 2012, or an auxiliary request (claims 1-3) filed as second auxiliary request with the grounds of appeal.

The further text on file is: description pages 1 and 24 filed with letter dated 6 July 2012; pages 2-7, 9-23 as originally filed; page 8 filed with letter dated 26 July 2007; drawing sheets 1-11 as originally filed.

IX. The sole independent claim of the main request reads as follows:

"1. An interface circuit for outputting serially a clock signal and data synchronized with said clock signal to a data register in response to a control signal (CE) changing from one level to the other level, said interface circuit comprising:

a first gate circuit (306, 308) for gating by said control signal (CE) said clock signal (clock signal input (CL) signal) to be output as a latch clock signal

(LCL);

a latch circuit (310) including an L (data) terminal, an R (reset) terminal, a C (clock) terminal, and a Q(output) terminal, a constant voltage (V) being applied to said L (data) terminal, said control signal (control signal input (CE) signal) being input to said R (reset) terminal, said latch clock signal (LCL) being input to said C (clock) terminal; and

a second gate circuit (312, 316) for gating by an output signal from said Q (output) terminal said clock signal (clock signal input (CE) signal) to be output as a clock signal output (SCL) signal,

characterized in that

at a time when said control signal (CE) changes from one level to the other level,

a reset state of said latch circuit is released and the level of said clock signal (clock signal input (CL) signal) at the time is detected, and

said constant voltage (V) is transferred to from said Q (output) terminal without delay, if said clock signal (clock signal input (CL) signal) is at one level, and

said constant voltage (V) is transferred to said Q (output) terminal after waiting until said clock signal (clock signal input (CL) signal) is at one level, if said clock signal (clock signal input (CL) signal) was at the other level."

In view of the outcome of the appeal the wording of the auxiliary request claims is immaterial.

Reasons for the Decision

1. *Original disclosure of the main request*

1.1 The examining division did not raise any objections under Article 123(2) EPC in its decision and the board concurs that there was no reason to do so with respect to the claims as refused.

1.2 The independent claim of the present main request has been significantly rewritten. As to the various amendments, the board finds that they satisfy the requirements of Article 123(2) EPC:

- *"for outputting serially a clock signal and data synchronised with said clock signal": see figures 1, 4;*
- *"in response to a control signal (CE) changing from one level to the other level": see original description page 13, paragraph 3 and page 14, lines 10-20;*
- *"a first gate circuit (306, 308) for gating by said control signal (CE) said clock signal (clock signal input (CL) signal) to be output as a latch clock signal (LCL);
a latch circuit (310) including an L (data) terminal, an R (reset) terminal, a C (clock) terminal, and a Q(output) terminal, a constant voltage (V) being applied to said L (data) terminal, said control signal (control signal input (CE) signal) being input to said R (reset) terminal, said latch clock signal (LCL) being input to said C (clock) terminal; and
a second gate circuit (312, 316) for gating by an output signal from said Q (output) terminal said*

clock signal (clock signal input (CE) signal) to be output as a clock signal output (SCL) signal,": see figures 1, 2;

- *"at a time when said control signal (CE) changes from one level to the other level, a reset state of said latch circuit is released and the level of said clock signal (clock signal input (CL) signal) at the time is detected"*: see page 13, paragraph 3 and page 14, lines 10-20;
- *"said constant voltage (V) is transferred to from said Q (output) terminal without delay, if said clock signal (clock signal input (CL) signal) is at one level, and"*: see figure 3;
- *"said constant voltage (V) is transferred to said Q (output) terminal after waiting until said clock signal (clock signal input (CL) signal) is at one level, if said clock signal (clock signal input (CL) signal) was at the other level."*: see figure 4.

1.3 As to new claims 2-4 of the main request, a basis for claim 2 can be found in description page 16, line 11 to page 17, line 14 and in figure 5 (this dependent claim was also in one of the claim sets on which the decision was based, and was not objected to under Article 123(2) EPC); a basis for claims 3 and 4 can be found in figure 1.

2. *Clarity*

2.1 In the appealed refusal decision, differentiating feature (b) ("to output clocks ... that are the same in number as bits of said data to said data register") of claim 1 of the then main request was objected as insufficiently disclosed in the sense of Article 83 EPC

(section 2.3). The reason was that none of the embodiments foresees means to adapt the number of clock pulses to the actual number of data bits to be transferred. The board agrees with the refusal that neither in claim 1 nor in the embodiments are there means that would ensure that feature (b) is present. It seems that (b) is more a *condition* than a feature. This condition fully depends on the *surrounding system* of the circuit of claim 1. However this is a question of clarity, rather than one of insufficient disclosure. At any rate, this feature has been removed from the claims, so that this objection (whether under Article 83 or 84 EPC) no longer arises.

2.2 Claim 1 of the current main request has also overcome the clarity objections raised by the board in the provisional opinion accompanying its summons to oral proceedings. However, this claim still contains two minor clarity problems:

- In line 30, the word "from" has no sense, since the constant voltage is transferred to the Q output terminal, and not "to from". Therefore, the "from" has to be deleted.
- In line 22, the clock signal input should be designated by (CL) like in line 12 and not by (CE).

3. *Inventiveness of main request*

3.1 As said above, claim 1 of the present main request has been significantly rewritten. However, the arguments of section 3 of the decision ("standard generic method", relating to the refused auxiliary request) still apply to this claim since the details which the current claim

has in addition to the refused one are already dealt with in section 3. For example, the newly added first gate circuit (306, 308) is motivated on page 9, step (5), point (d), and the inputs of the latch are dealt with in points (d)-(f). It is therefore necessary for the board to consider whether it finds convincing the reasons given by the examining division for finding the refused auxiliary request to be lacking an inventive step.

3.2 In contrast to the comparison of claim 1 of the then main request with document D1 (refusal, section 2.1), it is not clear which document had de facto been used as the closest prior art for claim 1 of the then auxiliary request. In section 3.1 it was stated that serial communication interfaces with data, clock and clock enable signals formed part of the prior art of the application as exemplified by documents D1-D3. In what follows, claim 1 seems to have been compared with D2 as closest prior art, since the objective technical problem was formulated as overcoming the disadvantages of D2 (sections 3.2, 3.3, 3.7).

3.3 There follows an explanation on almost three pages (7-10, sections 3.4, 3.5) of a "standard generic method" that the skilled person would apply when trying to tackle the problem. This method comprises six main steps of which step (4) has three sub-steps, and step (5) six.

In step (1), the prior art circuit of figure 10 of the application is analysed as a starting point. Thus, it seems that now the closest prior art is the circuit of figure 10 of the application, and not the interface circuit of D2.

In step (3), the "solution" of D2 with its unwanted delay is considered. In section 3.7, it is stated:

"Hence by the application of the standard method to the technical problem obviously resulting from the application of the teaching of D2 the man skilled in the art is forced to follow the above given one-way street."

3.4 In the grounds, it is assumed that the refusal started from D1 as the closest prior art. The objective technical problem solved is "that when the circuit of D1 is used with a variety of different controllers, different results occur when used with chips from different manufacturers" (page 2, paragraph 3). And further:

"In some chips, the clock output is low when the controllers are not operating, and in some the clock output is high."

This seems to correspond to the technical problem "how to avoid the output of a spurious clock signal" formulated in section 2.2, paragraph 1 of the refusal in the context of differentiating feature (a) of claim 1 of the then main request over D1.

3.5 The grounds continue by qualifying the above mentioned "standard method" as lengthy (page 2, second bold-faced heading). It started from nothing more than a black box in D1, labelled "Interface circuit" (page 3, paragraph 2; see D1, figure 4 for the interface circuit (12)). Document D2 is said to disclose "a configuration that operates irrespective of H-start or L-start of the clock input from an exterior" (page 3,

paragraph 3). Thus, the appellant seems to concede that D2 gives a solution to the above mentioned technical problem of avoiding spurious clock signals when using controllers with clocks starting high or low. However, the solution in D2 consisted in capturing all the data and thereafter determining "whether or not to abandon the first bit of the data according to the circumstances" (paragraph 3, last but one sentence; see D2, column 10, lines 18-33 for the functioning of the circuit of D2 in the presence of clocks starting high or low). On the other hand, the invention could "instantaneously detect whether the clock is H-start or L-start at the time when a control signal" changed.

3.6 The board considers D1 unsuitable to be the closest prior art. The reason is that D1 does not deal with the two types of controllers which stop (and re-start) the clock either on a high or a low level after a serial data transfer has been finished (called H-start and L-start by the appellant). In D1, the controller is of type L-start (see figure 5). Furthermore, D1 does not describe the structure of the interface circuit, it merely indicates the presence of that circuit as box (12) in figure 4 and describes its function in section [28] (essentially outputting clock CL as SCL and data DI as SDI after CE changed to high).

3.7 It is document D2 that deals with the two types of controllers (column 10, lines 21-33) and describes the structure of the interface circuit (part of figure 1). D2 assumes that an additional control data P is transmitted by the controller over the serial bus together with the data (column 10, lines 21-24). This control data P indicates whether the controller is of

type H-start or L-start. It is stored in latch (18) (see figure 1) and is used to fix the serial data input DT by the transistor (22) at low level in order to avoid it being input to the input data register (16) when the data is not yet ready.

Since D2 is the only one of the used documents D1-D3 that works with the two types of controllers, the board considers it as the closest prior art among the available documents.

Claim 1 has no feature in common with D2. It might seem that the AND-gate (17) of figure 1 in D2 would correspond to either the first gate circuit (306, 308) or the second gate circuit (312, 314). But the output of the first gate circuit is not connected with the data register, but with the latch (310) (which has no correspondence in D2). Such a connection with the data register is present in the second gate circuit (312, 314) (see signal SCL in figures 2 and 9), but the control signal CE is not (necessarily) an input of the second gate (see claim 1, lines 20-23 on page 26 as filed on 6 July 2012, and figure 2), in contrast to the AND-gate (17) of D2. Furthermore, the latter has an input INCO instead of the SCLEN signal from the latch (see D2, figure 1, AND-gate (17)).

The claimed invention does not have the control data P which D2 does. This omission makes the data transmission faster and allows the use of a simpler controller which does not send P.

Hence, the objective technical problem solved by the claim when compared with D2 can be formulated as

providing a faster and simpler interface circuit that also works with the two types of controllers.

One obvious solution would be that the interface circuit detects the controller type when the circuit is switched on for the first time, and stores the type once for all instead of receiving it during each data transfer. Then, the XOR-gate (27) and the other circuitry after it in figure 1 of D2 remains unchanged and can be driven with this stored type signal.

However the claimed invention solves the problem in a completely different way. It merely uses two AND-gates and one latch in order to mask the spurious clock pulse. The board therefore judges that the claimed invention is not obvious starting from document D2.

- 3.8 The only other plausible starting point would be the circuit of the dashed box in figure 10 of the application as the closest prior art. As mentioned above, this is the starting point of the alleged standard generic method in the examining division's decision (page 7, section 3.5, step (1)). This interface circuit merely consists in an AND-gate (104) with the clock signal (CL) and the control signal (CE) as inputs (again, there is no gate in the claim with the same connections). It only works correctly with an L-start controller (figure 11). When used with an H-start controller, it produces a spurious clock pulse (figure 12: "DUMMY CLOCK") which would cause the data register connected with the interface circuit (figure 9) to read in a wrong data bit (see also page 7, first paragraph).

The objective technical problem of claim 1 when compared with the circuit of the dashed box in figure 10 of the application would be to provide an interface circuit that works with both types of controller.

- 3.9 To solve this problem, the skilled person could try to apply the solution of D2 to the circuit in figure 10. However, this would not work with the same controllers. A controller which works with the circuit of D2 must transmit the additional control data P. The skilled person could accept the inconveniences of the solution of D2 or he could try to come up with a solution without the control data P, as in the claimed solution. In order to arrive at the latter, the skilled person would have to perform all the six steps and the nine sub-steps of the so-called standard generic method of the decision. No evidence has been put forward by the examining division to demonstrate that this method is really "standard". On the contrary, the board considers it very implausible that a skilled person would, without the exercise of inventiveness, perform exactly every step and sub-step in the described way to end up with the claimed circuit. Moreover, in the decision (sections 3.5 and 3.7) the standard generic method is compared to a one-way street, but it has multiple end points (namely at least using a latch or a flip-flop), as the appellant pointed out during oral proceedings (section 5.2). The examining division calls this an arbitrary selection. But this is not an arbitrary selection in replacing a feature of the closest prior art circuit to come up with the invention; it is an arbitrary selection in a hypothetical design process of which every step is meant to be deterministic. In fact,

at least this choice between latch and flip-flop is not deterministic, and therefore the skilled person is not "forced to follow the above given one-way street" (as formulated in section 3.7). The board is, in short, not convinced by the examining division's arguments with respect to this starting point.

3.10 Therefore, claim 1 of the main request is inventive in the sense of Article 56 EPC.

4. *Adaptations*

The board notes that claim 1 of the main request has to be amended according to section 2.2 (clarity) in order to be allowable. The description does not seem to need to be further adapted, amendments having been submitted with the letter dated 6 July 2012.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The application is remitted to the department of first instance for further prosecution on the basis of the main request filed with the letter dated 6 June 2011.

The Registrar:

The Chairman:

L. Fernández Gómez

D. H. Rees