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Case Number: T 2117/08 - 3.4.03

Application Number: 97108659.0

Publication Number: 810667

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Language of the proceedings: EN

Title of invention:
Triple well flash memory cell and fabrication process

Applicant:
HYUNDAI ELECTRONICS AMERICA, INC.

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 2117/08 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 7 March 2012

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 6 June 2008 refusing European patent application No. 97108659.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 97 108 659 for added subject-matter, lack of clarity and lack of novelty, Article 123(2) EPC, Articles 84 and 54(1) and (2) EPC 1973, (main request) over document

D2: US 5 457 652 A

and for lack of an inventive step, Article 56 EPC 1973, (first auxiliary request) over document D2 and documents

D4: US 5 491 657 A
D6: EP 0 690 508 A.

II. With the statement setting out the grounds of appeal, the appellant requested that the decision under appeal be set aside and a patent granted on the basis of the following:

Main request:

Claims 1 and 2 filed as main request with the statement setting out the grounds of appeal dated 15 October 2008;

Auxiliary request:

Claim 1 filed as auxiliary request with the statement setting out the grounds of appeal dated 15 October 2008.

III. Claim 1 according to the main request reads as follows:

"Method of operating a non-volatile memory cell comprising:
choosing a non-volatile memory device which comprises:
a semiconductor substrate (20) of first conductivity type (P) having a surface;
a first well region (22) disposed in the substrate (20) adjacent the surface thereof, the first well region (22) of second conductivity type (N) opposite to the conductivity of the first conductivity type (P);
a second well region (24) of the first conductivity type (P) disposed in the first well region (22) adjacent the surface;
a floating gate (29) overlaying the surface of the second well region (24), the floating gate (29) having a first end and a second end;
a control gate (21) disposed above the floating gate (29);
a drain region (26) provided at the first end of the floating gate (29); and
a source region (27) provided at the second end of the floating gate (29);
wherein erasing the memory device comprises applying a first negative potential to the control gate (21), disconnecting the source and drain regions (27, 26) from any potential source, applying a first positive potential to the first well region (22), and applying a second positive potential to the second well region (24) disposed within the first well region (22), choosing the same value for the applied first positive and second positive potentials, and
wherein programming the memory device comprises applying a third positive potential to the control gate

(21), and applying a fourth positive potential to the drain region (26),
characterised by
choosing the applied first negative potential as being between -3.0 and -9.0 volts and choosing the applied second positive potential as being between +3.0 and +9.0 volts; wherein the first positive potential is chosen as being between +3.0 and +9.0 volts; and
applying a second negative potential in the range of -2.0 to -4.0 volts to the second well region (24) during programming, whereby
choosing the third positive potential as being between +5.0 and +9.5 volts and choosing the fourth positive potential as being between +3.0 and +5.0 volts, and connecting the source region (27) and the first well region (22) to ground potential during programming."

IV. The appellant in substance provided the following arguments:

The separation in the decision under appeal of "erasing" and "programming", and referring to different state of the art, respectively, (in total three documents and general knowledge of the skilled person) seemed to be not correct. In particular, the features of the characterizing portion of claim 1 according to the main request could not be divided because the features related to each other with regard to the inventive idea of the present application to use low voltages for operating the non-volatile memory cell. Document D2 only mentioned a single way to operate the non-volatile memory cell in which very high voltages were used. All potentials according to the subject-

matter of the present application were lower in value than the potentials given in D2. The skilled person did not have any motivation why to deviate from the technical disclosure given in D2. Accordingly, the subject-matter of claim 1 was new and involved an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Amendments*

Claim 1 as amended is based on claims 1, 20 and 22 as originally filed and the description, page 10, table 1 and page 8, line 15 to page 9, line 31, as well as figures 2A, 2B.

Claim 2 is based on the description, page 9, lines 18 to 22 and page 10, table 1.

Accordingly, the amendments comply with Article 123(2) EPC.

2.2 *Novelty*

2.2.1 *Document D2*

2.2.1.1 Document D2 discloses a method of operating a non-volatile memory cell, the cell comprising, in the terms of claim 1,

a semiconductor substrate (40) of first conductivity type (P) having a surface;
a first well region (42) disposed in the substrate (40) adjacent the surface thereof, the first well region (22) of second conductivity type (N) opposite to the conductivity of the first conductivity type (P);
a second well region (44) of the first conductivity type (P) disposed in the first well region (22) adjacent the surface;
a floating gate (50) overlaying the surface of the second well region (44), the floating gate (50) having a first end and a second end;
a control gate (54) disposed above the floating gate (50);
a drain region (46) provided at the first end of the floating gate (50); and
a source region (48) provided at the second end of the floating gate (50) (cf figures 2A, 2C and corresponding description).

2.2.1.2 Erasing the memory device of D2 comprises applying a first negative potential (-10V) to the control gate (54), disconnecting the source and drain regions (48, 46) from any potential source, applying a first positive potential (+3V) to the first well region (42), and applying a second positive potential (+3V) to the second well region (44) disposed within the first well region (42), choosing the same value for the applied first positive and second positive potentials (column 4, lines 39 to 44).

According to D2 the (first and second) positive potential applied to the first and second well regions

is +3V and thus between +3.0 and +9.0 volts as per claim 1.

However, in D2 the (first) negative potential applied to the control gate is -10V and thus higher than between -3.0 and -9.0 volts as per claim 1.

2.2.1.3 Programming the memory device according to D2 comprises applying a third positive potential (+12V) to the control gate (54), and applying a fourth positive potential (+6.5V to +7V) to the drain region (46) (column 3, line 63 to column 4, line 1).

However, in D2 the (third) positive potential applied to the control gate is +12V and thus higher than between +5.0 and +9.5 volts as per claim 1.

Moreover, in D2 the (fourth) positive potential applied to the drain region is +6.5V to +7V and thus higher than between +3.0 and +5.0 volts as per claim 1.

Finally, in D2 during programming the first and second well regions as well as the source region are connected to ground potential, whereas according to claim 1 a second negative potential in the range of -2.0 to -4.0 volts is applied to the second well region, the first well region and the source region being connected to ground potential.

The subject-matter of claim 1 is, thus, new over document D2.

2.2.2 *Document D4*

2.2.2.1 *Figure 1 of D4*

In figure 1 of D4 a conventional cell is disclosed comprising,
a semiconductor substrate (12) of a first conductivity type (P) having a surface;
a floating gate (24) overlaying the surface of the substrate, the floating gate having a first end and a second end;
a control gate (26) disposed above the floating gate;
a drain region (14) provided at the first end of the floating gate; and
a source region (16) provided at the second end of the floating gate (cf figure 1 and corresponding description).

No first and second well regions as in claim 1 are provided in this memory cell.

The memory device is erased by applying a negative or ground potential to the control gate and a positive potential to the source region (column 1, line 66 to column 2, line 2).

Programming comprises applying a (third) positive potential (+9V) to the control gate and applying a (fourth) positive potential (+5V) to the drain region (cf figure 1 and column 5, lines 31 to 40). In D4 the (third) positive potential applied to the control gate is +9V and thus between +5.0 and +9.5 volts as per claim 1 and the (fourth) positive potential applied to the drain is +5V and thus between +3.0 and +5.0 volts

as per claim 1. Moreover, the source region is connected to ground as in claim 1.

However, in the memory cell of figure 1 of D4 during programming the substrate is connected to ground potential, whereas according to claim 1 a (second) negative potential in the range of -2.0 to -4.0 volts is applied to the second well region and the first well region is connected to ground potential.

2.2.2.2 *Figure 10 of D4*

In figure 10 of D4, an alternative memory cell is disclosed, comprising, in the terms of claim 1,
a semiconductor substrate (216) of first conductivity type (P) having a surface;
a first well region (214) disposed in the substrate (216) adjacent the surface thereof, the first well region (214) of second conductivity type (N) opposite to the conductivity of the first conductivity type (P);
a second well region (212) of the first conductivity type (P) disposed in the first well region (214) adjacent the surface;
a floating gate overlaying the surface of the second well region (212), the floating gate having a first end and a second end;
a control gate disposed above the floating gate;
a drain region provided at the first end of the floating gate; and
a source region provided at the second end of the floating gate (cf figure 10 and corresponding description).

In this alternative memory cell, erasing comprises applying a +6.5V to the drain region (zero volts to the control gate and source region) and -3V to the substrate (column 6, lines 41 to 49; figures 3 and 4), or
applying a +8.5V to the drain region, zero volts to the control gate and allowing the source region to float (drain-side erase) (column 7, lines 23 to 26), or
applying -8.5V/-9V to the control gate, +5V to the source region and allowing the drain region to float (standard source-side erase) (column 7, lines 44 to 48; column 7, line 64 to column 8, line 2),
whereas according to claim 1 both source and drain regions are allowed to float, a (first) negative potential between -3.0 and -9.0 volts is applied to the control gate and a positive potential between +3.0 and +9.0 volts is applied to the first and second well regions.

Programming, comprises in this case applying a +3V to the drain region (ground potential to the control gate and source region) and -6V to the substrate (column 6, lines 36 to 41; figure 4), or
zero volts to the control gate and drain region, -8.5V to the p-well, the source region being allowed to float (column 8, lines 25 to 35), or alternatively
applying +8.5V to the control gate and the source region, zero volts to the p-well (substrate) and the drain region being allowed to float (column 8, lines 36 to 42), or
applying +8.5V to the control gate and the drain region, zero volts to the p-well (substrate) and the source

region being allowed to float (column 8, lines 43 to 47).

Claim 1, on the other hand, requires for programming a (third) positive potential to the control gate between +5.0 and +9.5 volts, a (fourth) positive potential between +3.0 and +5.0 volts to the drain region, a (second) negative potential in the range of -2.0 to -4.0 volts to the second well region, and ground potential to the source region and the first well region.

2.2.2.3 Accordingly, the subject-matter of claim 1 is also new over document D4.

2.2.3 The subject-matter of claim 1 is also new over the remaining available, more remote prior art.

2.3 *Inventive step*

2.3.1 In the decision under appeal, it is held that the erase and programming conditions applied to the memory cell may only be applied separately, ie consecutively. Thus the invention consisted in an aggregation of separate erase and programming conditions without a possible combined interaction (reasons 11.2.1.3).

Accordingly, the decision under appeal starts from two different closest prior art documents for the erasing and the programming conditions, respectively.

2.3.2 It is noted that in the board's view it is questionable whether this approach is in fact correct. The erasing and programming actions are interrelated at least to

the extent that they form part of operating one and the same memory device equipped with specific means for generating the required potentials both for programming and erasing. Hence, starting from one prior art device would appear in fact more appropriate. Still, since the subject-matter is not obvious starting from the two different prior art documents for programming and erasing, respectively, as discussed below, it is all the less obvious starting from only one of the prior art documents for both programming and erasing.

2.3.3 As far as the conditions for erasing the memory device are concerned, reference is made in the decision under appeal to document D2.

As discussed above, the only distinguishing feature of claim 1 over D2 for erasing the memory device is the (slightly) lower voltage on the control gate being between -3.0 and -9.0 volts compared to the -10 volts employed for erasing in D2.

No inventive merit is to be attributed to selecting an only slightly lower voltage to be applied to the control gate during erasing compared to D2, in particular in view of the fact that larger voltages are in general more difficult to generate and handle, and thus the skilled person is generally inclined to use lower voltages where possible.

Reference is also made to document D6, disclosing erasing conditions ("channel erase") for a memory cell, comprising applying -8V to the control gate and +8V to the (p) well ("channel line"), corresponding to the

erasing conditions of claim 1 (D6, column 2, line 57 to column 3, line 3).

The claimed selection, thus, is obvious.

2.3.4 On the other hand, as far as the conditions for programming the memory device are concerned, reference is made in the decision under appeal to document D4.

The decision under appeal essentially hinges on the assertion that "*the adaptation of the Fig. 1 conditions for application in a dual well EEPROM involves only the determination of suitable well voltage conditions on the basis of those given in D4, Fig. 3 together with the appreciation that the dual well must be reverse biased, to enable operation of the memory*" (cf reasons 11.2.1.4).

There is, however, no suggestion in D4 or elsewhere to apply the negative p-well bias used in the embodiment of figure 3 of D4 to the programming conditions disclosed in figure 1. Document D4 rather discloses to replace the negative gate voltage in combination with a positive drain voltage and a zero substrate voltage of figure 1 by a zero gate voltage in combination with a zero drain voltage and a negative substrate voltage of figures 3 and 4.

2.3.5 In fact, according to D4, a "*drawback of the conventional programming technique arises from the fact that a relatively high field is generated between the drain and the substrate during programming (p-type substrate has 0 V applied and the n-type drain region is at +6 V). As a result, there may be caused high*

energy holes ("hot" holes generated by a so-called "impact ionization") to be formed at the surface portion of the channel near to the drain-to-substrate junction, thereby producing damage thereto so as to cause severe degradation in its performance and reliability" (column 2, lines 26 to 36).

Providing a negative substrate voltage would in fact further increase the field generated between the drain and the substrate, thereby amplifying the above-identified drawback and, thus, cannot be held to be obvious in the light of document D4.

Neither is it rendered obvious in this context by any of the remaining cited documents.

2.3.6 The programming conditions as claimed are also not obvious starting from document D2 as the closest prior art.

As discussed above, in D2 programming the memory device comprises the steps of applying +12V to the control gate (54), and applying +6.5V to +7V to the drain region (46), the first and second well regions, as well as the source region, being connected to ground potential.

There is nothing in D2 or elsewhere suggesting a reduction of the control gate potential combined with the application of a negative potential to the (p) well region as per claim 1.

2.3.7 Accordingly, having regard to the available state of the art, the subject-matter of claim 1 is not obvious

to a person skilled in the art and, thus, involves an inventive step (Article 56 EPC 1973).

2.4 Claim 2 is dependent on claim 1, providing further limitations. The subject-matter of this claim, therefore, also involves an inventive step.

3. The patent application as amended also meets the remaining requirements of the EPC, so that a patent can be granted on the basis of these documents.

4. Under these circumstances, the appellant's auxiliary request need not be considered.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

   Description: Pages 1 to 18 as originally filed;

   Claim: Claims 1 and 2 filed as main request with the statement setting out the grounds of appeal dated 15 October 2008;

   Drawings: Sheets 1/12 to 12/12 as filed with letter dated 4 August 1997.

Registrar: Chair:

S. Sánchez Chiquero G. Eliasson