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Datasheet for the decision of 6 August 2013

| Case Number: | т 0545/09 - 3.5.02 |
|---------------------|--------------------|
| Application Number: | 01121259.4 |
| Publication Number: | 1191686 |
| IPC: | H03G 3/30 |
| | |

Language of the proceedings: ΕN

Title of invention:

Method and circuit for controlling baseband gain

Applicant:

NEC Corporation

Headword:

Relevant legal provisions:

EPC Art. 56, 123(2)

Keyword:

"Inventive step - (yes) after amendment"

Decisions cited: _

Catchword:

_



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Beschwerdekammern

Boards of Appeal

Chambres de recours

Case Number: T 0545/09 - 3.5.02

D E C I S I O N of the Technical Board of Appeal 3.5.02 of 6 August 2013

| Appellant: | NEC Corporation |
|-------------|---------------------|
| (Applicant) | 7-1, Shiba 5-chome |
| | Minato-ku |
| | Tokyo 108-8001 (JP) |

| Representative: | Betten | & Resch | |
|-----------------|---------|-----------|------|
| | Theatin | erstrasse | 8 |
| | D-80333 | München | (DE) |

| Decision un | der appeal: | Decision of the Examining Division of the |
|-------------|-------------|---|
| | | European Patent Office posted on 16 October |
| | | 2008 refusing European patent application No. |
| | | 01121259.4 pursuant to Article 97(2) EPC. |

| Composition | of | the | Board: |
|-------------|----|-----|---------|
| Chairman: | | М. | Ruggiu |
| Members: | | G. | Flyng |
| | | Ρ. | Mühlens |

Summary of Facts and Submissions

I. The applicant's appeal concerns the examining division's decision to refuse European patent application 01 121 259.4.

> In the contested decision, the examining division considered each of the requests on file at the time (main request and two auxiliary requests) and found none to be allowable.

Concerning the main request and first auxiliary request, the examining division held that the amendments to the independent claims (main request claims 1 and 3, first auxiliary request claims 1 and 4) offended Article 123(2) EPC.

Concerning the second auxiliary request, the examining division did not raise objection under Article 123(2) EPC, but held that claim 1 lacked an inventive step over the prior art document D1: US 5 298 868, Article 56 EPC.

II. During the course of oral proceedings held before the Board on 6 August 2013 the appellant presented a new main request (claims 1 to 7) to replace the main request that had been filed with the grounds of appeal (letter dated 13 February 2009) and presented an amended description.

> The appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Claims:

 1 to 7 of the main request filed at the oral proceedings of 6 August 2013,

Description:

- pages 1 to 9, 9a, 9b and 10 to 20 filed at the oral proceedings of 6 August 2013,

Drawings:

- figure 2 filed with letter dated 17 November 2006,
- figure 1 and figures 3 to 10 as originally filed.
- III. Independent method claim 1 of the main request reads as follows:

"1. A gain control method for controlling a total amplifying gain of an output from a baseband amplifier including a plurality of series-connected variable gain amplifiers (102, 103, 104), by using a gain output value output from a gain converting circuit (113) the method comprising the steps of:

setting a prescribed gain change limit (MAXSTEP) for the total amplifying gain of said output from said baseband amplifier;

comparing a received gain input value with a gain output value currently set;

adding said prescribed gain change limit (MAXSTEP) to said currently set gain output value when said gain input value is higher than said currently set gain output value by said prescribed gain change limit (MAXSTEP) or more, or subtracting said prescribed gain change limit (MAXSTEP) from said currently set gain output value when said gain input value is lower than said currently set gain output value by said prescribed
gain change limit (MAXSTEP) or more;

waiting a predetermined time period; and

repeating the comparing step, the adding step or the subtracting step, and the waiting step until a difference between said gain input value and said currently set gain output value is smaller than said prescribed gain change limit (MAXSTEP), and then setting the gain output value to be equal to the gain input value."

Independent apparatus claim 4 of the main request corresponds to a large extent to independent method claim 1.

Claims 2, 3 and 5 to 7 are dependent claims.

IV. The appellant argues in essence that claim 1 of the main request does not add subject-matter contrary to Article 123(2) EPC and is novel and inventive over the cited prior art.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments, Articles 123(2) EPC

2.1 To a large extent, the set of claims 1 to 7 of the main request corresponds to the set of claims 1 to 7 of the second auxiliary request considered in the contested decision. In that version, the final feature of independent claim 1 reads (emphasis added):

> "repeating the comparing step <u>and</u> the adding step or the subtracting step and the waiting step until a difference between said gain input value and said currently set gain output value is smaller than said prescribed gain change limit (MAXSTEP), <u>in which case</u> the gain output value <u>is set</u> to be equal to the gain input value".

Independent claim 1 of the main request differs in that this feature reads (emphasis added):

"repeating the comparing step, the adding step or the subtracting step, and the waiting step until a difference between said gain input value and said currently set gain output value is smaller than said prescribed gain change limit (MAXSTEP), <u>and</u> <u>then setting</u> the gain output value to be equal to the gain input value.

Independent apparatus claim 4 has been amended in the same manner as claim 1.

2.2 Whereas it might have been possible to interpret the phrase "in which case the gain output value is set to

be equal to the gain input value" as a mere description of the status that is deemed to exist upon reaching the specified condition that the difference between the gain input value and the currently set gain output value is smaller than the prescribed gain change limit (MAXSTEP), the amended phrase "and then setting the gain output value to be equal to the gain input value" makes it clear that this is an actual step of the method that is carried out when the specified condition is reached. This is consistent with the disclosure of figure 2, from which it is evident that step S3 is a step of the method, and also with the disclosure of figure 3, from which it is evident that at time t_1 the gain output is set to the same level as the gain input (see also the corresponding portion of the description in paragraph [0064] of the application as published, EP 1 191 686 A2).

2.3 The examining division did not raise any objection under Article 123(2) EPC to the amendments made according to the then second auxiliary request. The Board sees no reason to find otherwise and, for the reasons set out above, sees no reason to object to the further amendments that have been made according to the present main request.

3. Novelty and inventive step

3.1 Document D1 may be considered to be the closest prior art. It discloses in the embodiment of figure 3 and the associated description a gain control amplifier that includes three variable gain amplifiers 15, 19, 22 that are connected in series. Each amplifier has a control input terminal that is connected to the output of a respective D/A converter 16, 20, 23 and each D/A converter receives a digital input signal from a respective up-down counter 17, 21, 24 (cf. column 4, lines 47 to 63).

As set out in the paragraph spanning columns 4 and 5, a clock input terminal of the first up-down counter 17 is connected to a clock signal input terminal 18. Outputs C1 and C2 from the first and the second up-down counters 17 and 21 are coupled to clock input terminals of the second and the third up-down counters 21 and 24, respectively. Counting direction control terminals of the first, the second and the third up-down counters 17, 21 and 24 are commonly connected to a control signal input terminal 25.

The original signal is amplified with the gain (in decibels) of the gain control amplifier 201, which is a sum of the gains of the first, the second and the third gain control amplifiers 15, 19 and 22, and is outputted at the signal output terminal 11 (see column 5, lines 8 to 12).

According to column 5, lines 13 to 18, in this embodiment, the gain of the first gain control amplifier 15 is increased first, that of the second gain control amplifier 19 is increased next, and that of the third gain control amplifier 22 is increased at last until a desired gain of the gain control amplifier 201 is reached. To decrease the gain of the gain control amplifier 201, the gains of the first, the second and the third amplifiers 15, 19 and 22 are decreased in the reverse order of the increase of the gain (cf. dependent claims 3 and 7 of the appellant's main request).

The detailed operation of the gain control amplifier is described from column 5, line 22, where it is stated:

"If a desired gain of the gain control amplifier 201 is larger than a sum of the gains of the first, the second and the third gain control amplifiers 15, 19 and 22, the gain of the first gain control amplifier 15 starts to increase. More precisely, up-down clocks are given to the first, the second and the third up-down counters 17, 21 and 24 so as to set the up-down counters to count up. Next, gain control clocks are supplied to the first up-down counter 17 one after another and counted therein. A count registered by the first up-down counter 17 is given to the first D/A converter 16 as the first output S1. The second output C2 has not been given to the second up-down counter 21 yet at this stage. The first output S1 in digital form is converted into an analog signal in the first D/A convertor 16 and transmitted to the control input terminal of the first gain control amplifier 15.

Thus, the gain of the gain control amplifier 201 initially increases with an increase in the gain of the first gain control amplifier 15.

If the operation as above has yielded the desired gain of the gain control amplifier 201, supply of the gain control clocks is cut off. On the contrary, if the desired gain has not been reached even with the first output S1 representing that the first up-down counter 17 has registered a full count, the gain control clock is given to the second up-down counter 21 as the second output C1 while the first output S1 continues to represent the full count registered at the first updown counter 17. The second output C1 makes the second up-down counter 21 count as the first up-down counter 17 does. Thus, the gain of the second gain control amplifier 19 increases in accordance with the first output S2 obtainable at the second D/A converter 20.

In other words, the gain of the second gain control amplifier 19 starts increasing only after the gain of the first gain control amplifier 15 has reached its maximum. The same is true of the relationship between the gains of the second and the third gain control amplifiers 19 and 22."

D1 further discloses that:

"... the gain of the gain control amplifier 201 increases as the gain control clocks supplied to the up-down counters increase in number, i.e., as a clock count increases" (see column 6, lines 9 to 12); and

"... if a decrease in the gain of the gain control amplifier 201 is desired, the up-down clocks set the first, the second and the third up-down counters 17, 21 and 24 to count down. In this case, an increasing clock count causes the gain of the gain control amplifier 201 to decrease" (see column 6, lines 31 to 36).

3.2 The appellant argues that document D1 does not disclose setting a prescribed gain change limit (MAXSTEP) for the total amplifying gain of the output from the baseband amplifier (cf. independent claims 1 and 4).

> In the contested decision (see section 3.1) the examining division held that in D1 the gain change limit was defined by the setting of the gain change per one up or down counting step.

The Board considers that the person skilled in the art reading document D1 would realise that each up or down count of one of the up-down counters would cause a discrete change in the analogue output of the corresponding D/A converter, which would result in a step change in the gain of the corresponding gain control amplifier, causing a corresponding step change in the total amplifier gain. The amount of the step change in gain per clock cycle would be determined by the control characteristics of the three gain control amplifiers, which are shown in figures 4 and 5 (see also column 6, lines 38 to 58).

Whilst D1 does not refer explicitly to "setting a prescribed gain change limit", the Board considers that in any given clock cycle the change in total amplifier gain would be limited to an amount that is determined by the amplifier characteristics. When the amplifier characteristics are selected for a particular application this could be considered as "setting a prescribed gain change limit" as claimed.

3.3 The appellant also argues that document D1 does not anticipate any of the further method steps (comparing, adding, waiting and repeating steps) according to claims 1 and 4.

It is derivable from document D1 that:

- if the desired gain of the gain control amplifier is larger than a sum of the gains of the individual gain control amplifiers, the counters are set to count up and control clocks are supplied to increase the total gain of the amplifier; - conversely, if the desired gain of the gain control amplifier is smaller than a sum of the gains of the individual gain control amplifiers, the counters are set to count down and control clocks are supplied to decrease the total gain of the amplifier;

 if this yields the desired gain of the gain control amplifier, supply of the gain control clocks is cut off.

In order to decide which of these conditions exists, it seems to the Board that it would be obvious, and might even be necessary, to compare the desired gain (received gain input value) with the total amplifier gain (gain output value currently set). Furthermore, if the supply of the gain control clocks is to be cut off when the desired gain of the gain control amplifier is reached, it would seem to be necessary to wait and then repeat that comparison in each period between successive gain control clocks. As already set out, it seems that each gain control clock supplied to one of the counters would cause a step change in gain (prescribed gain change limit) to be added to, or subtracted from, the currently set gain output value.

According to claims 1 and 4, the prescribed gain change limit is added to (or subtracted from) the currently set gain output value when the gain input value is higher than (or lower than) the currently set gain output value "by said prescribed gain change limit (MAXSTEP) or more" and this is repeated "until a difference between said gain input value and said currently set gain output value is smaller than said prescribed gain change limit (MAXSTEP)". In document D1 there is no suggestion that when deciding whether or not to cut off the supply of clocks account could be taken of whether the difference between the desired gain and the actual total amplifier gain is smaller than the step change in gain that would be caused by applying the next clock pulse. However, the Board agrees with the examining division (see reasons for the decision, page 5, last paragraph) that this would be an obvious criterion for the skilled person to use for cutting off the supply of clock pulses.

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3.4 Finally, the appellant argues that document D1 does not disclose or render obvious the final feature of claim 1 (and the corresponding feature of claim 4) of "<u>setting</u> <u>the gain output value to be equal to the gain input</u> <u>value</u>" when the criterion is reached that the difference between the gain input value and the currently set gain output value is smaller than the prescribed gain change limit.

Here the Board does agree with the appellant, for the following reasons.

In document D1 the total amplifier gain can only be changed by applying clock pulses. As set out above, the amount of the step change in gain that is made per clock cycle is determined by the control characteristics of the three gain control amplifiers and is fixed. Hence, with the arrangement disclosed in D1 there is no possible way of setting the total amplifier gain to the desired gain when the difference between the desired gain and the actual total amplifier gain is smaller than the step change in gain per clock cycle. In the context of the present invention, in which changes in gain are carried out in steps of limited magnitude with pauses in between to reduce undesirable transient effects, this additional feature has the effect of allowing a final (smaller) adjustment of the gain to be made to make it equal to the desired gain. This solves the problem of increasing the accuracy of the final gain value of the amplifier.

Faced with this problem the claimed solution would not be obvious when starting from document D1 because it is not technically feasible with the arrangement disclosed.

None of the other documents cited in the search report is more relevant that document D1.

For these reasons the Board concludes that the subjectmatter of claims 1 and 4 is not obvious in view of the cited prior art. The remaining claims also meet the requirements for inventive step at least through their dependency on claims 1 or 4.

- 4. The description has been amended to acknowledge the prior art disclosed in document D1 and to render it consistent with the claims of the main request.
- In view of the above the board accedes to the appellant's request for grant.

Order

For these reasons it is decided that:

- 1. The decision under appeal is set aside.
- 2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Claims:

 1 to 7 of the main request filed at the oral proceedings of 6 August 2013,

Description:

- pages 1 to 9, 9a, 9b and 10 to 20 filed at the oral proceedings of 6 August 2013,

Drawings:

- figure 2 filed with letter dated 17 November 2006,
- figure 1 and figures 3 to 10 as originally filed.

The Registrar:

The Chairman:

U. Bultmann

M. Ruggiu