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**Datasheet for the decision
of 19 March 2013**

Case Number: T 1426/09 - 3.4.03

Application Number: 00988041.0

Publication Number: 1342271

IPC: H01L 29/24

Language of the proceedings: EN

Title of invention:

Method of fabricating a self-aligned bipolar junction transistor in silicon carbide and resulting devices

Applicant:

CREE, INC.

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 123(2)

Relevant legal provisions (EPC 1973):

EPC Art. 56, 84

Keyword:

"Clarity, support by description (no) - main request"
"Inventive step (no) - first auxiliary request"

Decisions cited:

G 0010/93

Catchword:

-



Case Number: T 1426/09 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 19 March 2013

Appellant: CREE, INC.
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Representative: Cross, Rupert Edward Blount
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 19 February 2009
refusing European patent application
No. 00988041.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
T. Karamanli

Summary of Facts and Submissions

- I. This is an appeal against the refusal of application No. 00 988 041 for lack of clarity and support by the description, Article 84 EPC (main and first auxiliary request then on file), and for added subject-matter, Article 123(2) EPC (second auxiliary request then on file).
- II. The appellant requested at oral proceedings before the board that the decision under appeal be set aside and that a patent be granted on the basis of the claims according to the main request, filed with letter of 19 February 2013, or according to the first auxiliary request, filed during oral proceedings of 19 March 2013 at 11:45 hours, or as a second auxiliary request in the following version:
- Claims 1 to 8 according to the second auxiliary request filed during the oral proceedings of 19 March 2013;
 - Description pages: 1, 8 to 11, as published; 2 to 7 and 12 to 13, filed during oral proceedings of 19 March 2013;
 - Drawing sheets: 1/8 to 8/8 as published.
- III. Claim 1 according to the main request reads as follows:

"A method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure (1, 11) having a first layer (6) of silicon carbide and a second layer (7, 8) of silicon carbide, the method comprising:

forming a trench (14) in the second silicon carbide layer, the trench having a bottom wall (14B) and opposing side walls (14A);

depositing a spacer layer (18) having a predetermined thickness on the second silicon carbide layer, including the bottom wall and side walls of the trench; anisotropically etching the spacer layer from a portion of the bottom wall of the trench between the side walls, thereby exposing a portion of the bottom wall of the trench while at least a portion of the spacer layer remains on the side walls;

doping a region (20) below the exposed portion of the bottom wall with a dopant to create a doped well region below the bottom wall; and

removing the portion of the spacer layer remaining on the sidewalls."

IV. Claim 1 according to the first auxiliary request reads as follows:

"A method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure (1, 11) having a first layer (6) of silicon carbide and a second layer (7, 8) of silicon carbide, the method comprising:

forming a cap layer (10) on the second layer of silicon carbide;

etching the cap layer and the second silicon carbide

layer to form a plurality of pillars (12) defining at least one trench therebetween, each trench having a bottom wall (14B) and opposing side walls (14A); depositing a spacer layer (18) having a predetermined thickness on the second silicon carbide layer, including the bottom wall and side walls of each trench; anisotropically etching the spacer layer from a portion of the bottom wall of each trench between the side walls, thereby exposing a portion of the bottom wall of each trench while at least a portion of the spacer layer remains on the side walls; doping a region (20, 21) below the exposed portion of the bottom wall with a dopant to create a doped well region below the bottom wall in the first layer; and removing the portion of the spacer layer remaining on the sidewalls; and wherein either the first layer (6) and the second layer (8) comprise a base region and the well region (20) comprises an emitter region or the second layer (7) comprises an emitter region and the well region (21) and the first layer (6) comprise a base region."

V. Claims 1 and 8 according to the second auxiliary request read as follows:

*"1. A method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure (1, 11) having a first layer (6) of silicon carbide and a second layer (8) of silicon carbide, the method comprising:
forming a cap layer (10) on the second layer of silicon carbide;*

etching the cap layer and the second layer of silicon carbide (8) to form a pillar (12) having a first surface opposite the first layer of silicon carbide (6) and side walls, and a horizontal surface adjacent the pillar;

depositing a spacer layer (18) having a predetermined thickness on the first surface of the pillar, the side walls and the horizontal surface adjacent the pillar;
anisotropically etching the spacer layer from the horizontal surface adjacent the pillar while at least a portion of the spacer layer remains on the side walls of the pillar, thereby exposing the horizontal surface;
doping a portion (20) of the first layer of silicon carbide below the exposed portion of the horizontal surface with a dopant to create a doped well region in the first layer; and

removing the portion of the spacer layer remaining on the sidewalls; and

wherein the first layer (6) and the second layer (8) form a base region and the well region (20) forms an emitter region."

"8. A bipolar junction transistor fabricated in silicon carbide, comprising:

a substrate (2, 4) having a first conductivity type, having a top surface and a bottom surface and forming a collector region of the transistor;

an epitaxial layer (6) of silicon carbide deposited above the substrate, having a second conductivity type opposite the first conductivity type; and

a pillar (12) having a top wall and side walls formed above the epitaxial layer, the pillar forming part of a base region of the transistor, characterised by a doped well region (20) in the epitaxial layer

adjacent the pillar, a distance from the pillar of between 0.05 and 0.5 μm , the doped well region having the first conductivity type and forming the emitter region of the transistor."

VI. Reference is made to the following documents:

D1: WO 00 74129 A

D2: US 4 945 394 A

D3: US 5 424 227 A

D4: WO 91 07778 A

VII. The appellant in substance provided the following arguments:

Claim 1 of the main request met the requirements of Article 84 EPC. In particular, it was not necessary to define the exact location of the emitter and base regions, since the skilled person would immediately be able to see them in the completed device. Moreover, it did not appear that the formation of a pillar consisting of a portion of the second silicon carbide layer was essential to the invention, because the definition of a trench on its own provided the skilled person with a clear understanding of the structure to be formed. The cap dielectric layer was also not an essential feature of the invention.

The issues relating to inventive step and particularly based on document D3 had not been raised previously. On

this basis, it was requested that the case be remitted to the examining division.

Moreover, document D3 was not concerned with silicon carbide and the doped well region was not provided at the bottom of a trench between two pillars and thus not bound on one side. As indicated in the description, the precision with which the base and emitter regions could be spaced using photolithographic techniques was limited, which could result in undesirably high base resistance and unwanted base-collector capacitance, both of which reduced the ability of the device to operate at high frequencies. A synergistic effect was provided by the use of silicon carbide and the tight control of the dimensions of the base and the base-emitter spacing, making the device capable of operating at higher frequencies. As there was no suggestion in D3 to increase the frequency range, there was no reason to turn to silicon carbide. Moreover, there was no evidence on file of an emitter region consisting of a plurality of pillars being known to the skilled person. Document D1 did not concern silicon carbide and provided a collector-up transistor. Document D2, disclosed a silicon carbide transistor, however without a trench. Thus, the skilled person would not arrive at the invention starting from document D3 or D2.

Accordingly, the invention comprised an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Amendments*

Claim 1 as amended according to the main request is based on claim 1 as originally filed and on the description as originally filed, page 10, lines 31 to 32 and figure 6, specifying that the portions of the spacer layer remaining on the sidewalls are removed.

Accordingly, the amendments to claim 1 comply with Article 123(2) EPC.

2.2 *Article 84 EPC 1973*

2.2.1 The appellant's main request corresponds to the main request on file before the examining division, refused for lack of clarity and support by the description.

2.2.2 According to the application, "*It is an object of the present invention to enable precise and close spacing of the base and emitter contacts in a bipolar junction transistor formed in silicon carbide*" (page 3, lines 28 to 29).

Claim 1 is directed at a method of fabricating a self-aligned bipolar junction transistor, however, fails to define which parts form the base and emitter regions. Yet, in order to attain the above object of the invention, the spacing between the base and emitter of the transistor must be apparent from the claim, which requires that the base and emitter regions be defined.

The appellant argued that the presence of emitter, base and collector regions was implicit from the fact that a bipolar junction transistor was being formed. Accordingly, there was no need to specify these regions.

In the board's judgement, however, although it can be accepted that the collector region in the present case need not be specified, a clear definition of which parts form the base and emitter regions so that the spacing between those regions is apparent from the claim is required, as discussed above.

2.2.3 In the decision under appeal, the reference in claim 1 to a (single) trench as well as the failure to define a pillar was considered to render the claim unclear and not supported by the description.

A "trench" only defines the gap between two adjacent pillars of one device, but not the remaining outer periphery of each of the pillars where no opposing sidewalls and, thus, no "trench" is present (see eg figure 3A). The formation of a (single) trench is, thus, not sufficient to define a pillar formed from the second layer. The formation of a pillar from the second layer, however, is essential as it forms either the base or the emitter region of the transistor, the definition of which is considered essential as discussed above. In fact, as disclosed in the description, "*portions of the oxide layer 10 and layer 8 are etched away to form pillars 12*", "*each pillar 12 comprises a raised portion 16 formed from layer 8 and a cap portion 13 formed from oxide layer 10*" and "*pillars 12 define trenches 14 having bottom walls 14B along the surface 6B of layer 6 and side walls 14A*" (page 8,

lines 24 to 31). Moreover, "*Raised portions 16 will ultimately define the base region in the completed BJT device*" (page 8, lines 31 to 32).

The appellant essentially argued that since claim 1 explicitly required the trench to have a bottom wall and opposing sidewalls, such a structure could only represent a gap between adjacent pillars. The remaining outer periphery of a pillar where no opposing sidewall was present was already excluded from the definition of a trench in accordance with claim 1. On that basis, it did not appear that the formation of a pillar consisting of a portion of the second silicon carbide layer was essential to the invention, because the definition of a trench on its own provided the skilled person with a clear understanding of the structure to be formed.

In the board's judgement, however, since, as conceded by the appellant, the remaining outer periphery of a pillar is excluded from the definition of a trench in accordance with claim 1, claim 1 fails to define a pillar formed from the second layer, essential for defining the base or emitter region it ultimately forms.

2.2.4 Finally, forming a cap layer on the second layer of silicon carbide is considered to be essential to the performance of the invention. In particular, as is apparent from the description, this layer (10) protects the pillar (p++ and n++, respectively) formed from the second layer of silicon carbide (7, 8) during the doping (n+ and p+, respectively) of the self-aligned well regions (20, 21).

The appellant disagreed that the cap dielectric layer was an essential feature of the invention. Although it might be true that this layer could protect the heavily doped silicon carbide layer during the implant of the self-aligned regions, this was never explained as being essential to the fabrication of the device in the application. Moreover, such a protective function could be performed in a wide range of alternative ways, such as by adding a metal layer.

The board cannot agree. A feature need not be explicitly specified in the application as being essential to the invention to be so. Decisive is whether to a skilled person reading the application, the feature is understood to be necessary for attaining the object of the invention, that is to solve the problem posed. In the present case, when doping the well region, the pillar formed from the second layer, which is oppositely doped, must not be counter doped. To this end, a cap oxide layer is formed on the second layer according to the application. No other solution is offered in the application or can be held to be readily apparent to the skilled person. Only insofar as the material of this cap layer is concerned, it can be accepted that the skilled person would understand oxide not to be essential in that other materials could be suitable as well.

- 2.2.5 Since claim 1 does not contain the features discussed above it does not meet the requirement following from Article 84 EPC 1973, taken in combination with Rule 29(1) and (3) EPC 1973, that any independent claim must contain all the essential features of the

invention (cf Case Law of the Boards of Appeal of the EPO, 6th edition, II.B.1.1.4).

Accordingly, the appellant's main request is not allowable.

3. *First auxiliary request*

3.1 *Amendments*

Claim 1 as amended according to the first auxiliary request is based on claims 1, 2 and 3 as originally filed and on the description as originally filed, page 8, line 16 to page 9, line 4 and figures 2, 3, 3A and 12 for the formation of the cap layer and the plurality of pillars defining at least one trench, and on page 8, line 8, page 10, lines 6 to 7, page 12, line 26 to 31, and figures 10 and 13 to 15 for the definition of the base and emitter regions.

Accordingly, the amendments to claim 1 comply with Article 123(2) EPC.

3.2 *Article 84 EPC 1973*

Moreover, claim 1 of the first auxiliary request contains the essential features of the invention, in particular those discussed above with respect to claim 1 of the main request, so that the requirements of Article 84 EPC 1973 are considered to be met.

3.3 *Request for remittal*

3.3.1 In the annex to the summons to oral proceedings, in addition to the issues above concerning Article 84 EPC 1973, the board also provided its provisional opinion on the issue of inventive step in particular by also referring to document D3.

3.3.2 The appellant argued in this respect that "*the issues relating to inventive step and particularly based on US-5,424,227 have not been raised previously. This is the first time that this document has been relied upon in relation to an objection. On this basis, I request that the case be remitted to the examining division for their consideration, in accordance with Article 111(1) EPC. It would be inequitable for the Applicant, appealing refusal of the application on the basis of clarity and support issues to begin a discussion regarding inventive step only at this late stage of the Appeal Procedure. At this stage, amendments are governed by the Rules of Procedure of the Board of Appeal (particularly Article 13) which are more restrictive than possible at first instance*".

3.3.3 Remittal of the case to the examining division lies at the discretion of the board (Article 111(1) EPC 1973). In deciding on the appellant's request, the board has to take due account of the particular circumstances of the case, thereby taking *inter alia* into consideration whether a decision by the board would speed up the proceedings significantly (cf G 10/93, OJ EPO 1995, 172; Reasons, point 5).

In the present case, in the proceedings before the examining division the objections of lack of clarity and support by the description, Article 84 EPC 1973, and added subject-matter, Article 123(2) EPC, notably concerning the trench and pillar, stood in the foreground, novelty and inventive step, with reference to documents D1 and D4, only being mentioned in passing.

Oral proceedings before the examining division were arranged in order to discuss these objections under Articles 84 EPC 1973 and Article 123(2) EPC. The applicant, however, did not attend the oral proceedings, thereby precluding further progress being made in the case on these objections and possibly the issue of novelty and inventive step being discussed before the examining division.

In appeal, in essence, the same objections were raised by the board, and only after appropriate amendments were made, the issue of novelty and inventive step was addressed in the end.

In view of the above, the general interest of the public in swift decisions on pending applications and the need for procedural economy must prevail.

Moreover, document D3 was cited in the international search report pertaining to the application in suit and, thus, was known to the appellant from the onset. Furthermore, the appellant was informed in the communication annexed to the summons to oral proceedings before the board, issued over five months prior to the oral proceedings, of the possible relevance of this document on the issue of inventive

step in the pending case, leaving the appellant with sufficient opportunity to take appropriate action.

Accordingly, the appellant's request for remittal is refused.

3.4 *Novelty*

3.4.1 *Document D3*

Document D3 discloses, in the terms of claim 1, a method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure having a first layer (4) and a second layer (6) of semiconductor material, the method comprising:

forming a cap layer (11) on the second layer;

etching the cap layer and the second layer to form a pillar;

depositing a spacer layer (12) having a predetermined thickness on the second layer;

anisotropically etching the spacer layer;

doping a region with a dopant to create a doped well region (7) in the first layer; and

removing the portion of the spacer layer remaining on the sidewalls; and

wherein the second layer (6) comprises an emitter region and the well region (7) and the first layer (4) comprise a base region (column 3, line 49 to column 4, line 25; figures 2 to 5).

The subject-matter of claim 1 differs from document D3, in that the semiconductor material of the first and second layer is silicon carbide whereas in D3 silicon-germanium and silicon is used. Moreover, according to

claim 1 a plurality of pillars defining a trench therebetween is formed whereas in D3 only one pillar (per transistor of the array) is shown.

Moreover, the alternative provided in claim 1 wherein the first layer and the second layer comprise a base region and the well region comprises an emitter region is not disclosed in D3.

Accordingly, the subject-matter of claim 1 according to the first auxiliary request is new over document D3 (Article 54(1) EPC 1973).

3.4.2 *Document D2*

Document D2, cited in the application as filed (cf description, page 2, line 33 to page 3, line 11), discloses a method of fabricating a silicon carbide bipolar junction transistor (cf D2, column 6, lines 6 to 45; figure 2).

The method, however, does not form a self-aligned transistor and in particular it does not comprise the steps of forming a spacer layer, anisotropically etching this layer to leave portions on the side walls of the emitter (pillar) followed by doping to create a doped well region forming part of the base of the transistor.

It is noted that in another embodiment of D2 shown in figure 3, the emitter is formed as a doped well. In this case, however, no pillar is provided forming part of the base. Accordingly, the alternative provided in claim 1 wherein the first layer and the second layer

comprise a base region and the well region comprises an emitter region is also not disclosed in D2.

Accordingly, the subject-matter of claim 1 is also new over document D2 (Article 54(1) EPC 1973).

3.4.3 Document D1

Document D1 discloses, a method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure having a first layer (5) and a second layer (6, 7) of semiconductor material, the method comprising: forming a cap layer (8) on the second layer; etching the cap layer and the second layer to form a plurality of pillars; forming sidewall spacers (10) on the sidewalls of the pillars; doping regions with a dopant to create doped well regions in the first layer; wherein the well regions and the first layer (5) comprise a base region (page 6, line 19 to page 8, line 22 and page 9, lines 8 to 28; figures 6 to 10 and 12).

The subject-matter of claim 1 differs from document D1, in that the semiconductor material of the first and second layer is silicon carbide whereas in D1 silicon-germanium and silicon is used. Moreover, according to claim 1, where the well region comprises a base region, the second layer comprises an emitter region, whereas in D1 the second layer (plurality of pillars) forms the collector of the transistor.

Accordingly, the subject-matter of claim 1 is also new over document D1 (Article 54(1) EPC 1973).

3.4.4 *Document D4*

Document D4 also discloses a method of fabricating a self-aligned bipolar junction transistor in a semiconductor structure.

The subject-matter of claim 1 differs from document D4, in that the semiconductor material of the first and second layer is silicon carbide whereas in D4 the semiconductor material is (poly)silicon. Moreover, according to claim 1 a plurality of pillars defining a trench therebetween is formed whereas in D4 only one pillar (per transistor) forming the emitter is shown.

Moreover, the alternative provided in claim 1 wherein the first layer and the second layer comprise a base region and the well region comprises an emitter region is also not disclosed in D4.

Accordingly, the subject-matter of claim 1 according to the first auxiliary request is also new over document D4 (Article 54(1) EPC 1973).

3.5 *Inventive step*

3.5.1 Claim 1 of the first auxiliary request covers two alternatives, a first in which the first layer (6) and the second layer (8) comprise a base region and the well region (20) comprises an emitter region (ie the first embodiment provided in the description; figures 1 to 10 and 14), and a second in which the second layer

(7) comprises an emitter region and the well region (21) and the first layer (6) comprise a base region (ie the second embodiment provided in the description; figures 11 to 13 and 15).

In the following, the second of these alternatives is considered.

3.5.2 The closest prior art is considered to be provided by document D3.

As discussed above for novelty, having regard to this alternative, the subject-matter of claim 1 differs from document D3 in that

- the semiconductor material of the first and second layer is silicon carbide whereas in D3 silicon/silicon-germanium is used, and
- a plurality of pillars defining a trench therebetween is formed whereas in D3 only one pillar is shown.

3.5.3 The technical effect of using silicon carbide compared to silicon/silicon-germanium is that the bipolar junction transistor has the capability of operating at higher temperatures, higher speeds and higher power levels (cf eg document D2, column 1, lines 53 to 67).

The plurality of pillars defining a trench therebetween, notably where the pillars form the emitter region and well regions in the trenches form the base region form what is commonly known as an interdigitated emitter-base structure. As is part of the common general

knowledge of a skilled person working on the technical field at issue in the present case of bipolar junction transistors, because of the voltage drop across the base-emitter junction, the emitter current tends to flow near the periphery of the emitter. The current-carrying capability is, therefore, proportional to the emitter periphery. In high-frequency transistors, requiring small area emitters to reduce junction capacitance, a commonly adopted solution is to provide several emitter stripes separated by interspersing base contact regions thereby increasing the useful length of the emitter periphery.

The technical effect of the formation of a plurality of pillars forming the emitter is, thus, that the bipolar junction transistor has the capability of operating at higher frequencies.

- 3.5.4 In view of the above, the objective problem to be solved relative to D3 is to make the transistor suitable for higher frequencies.

The claimed solution is to use silicon carbide as the semiconductor material for the transistor and to form a plurality of pillars defining at least one trench therebetween, which is essentially an interdigitated structure of pillars from the second layer forming the emitter region, separated by interspersing doped well regions forming the base contact regions.

As discussed above, from document D2 it is known that silicon carbide allows for higher operating frequencies. Accordingly, it would be obvious to the person skilled

in the art to use silicon carbide in the method of D3 as the semiconductor material.

Moreover, as discussed above, it is common general knowledge for the person skilled in the art of bipolar junction transistors that an interdigitated base-emitter geometry also allows for higher operating frequencies. Reference is made in this respect to document D1, showing a high-frequency power bipolar junction transistor, though in a collector-up configuration, with, for analogous reasons, an interdigitated geometry with a plurality of pillars and interspersed self-aligned doped well regions forming part of the base.

Accordingly, it would be obvious to the person skilled in the art to provide an interdigitated geometry by forming a plurality of pillars from the second layer in D3 as emitter, the pillars defining at least one trench therebetween, each trench having a bottom wall and opposing side walls with the spacer layer remaining on these side walls, and the doped well region created below the bottom wall of the trench in the first layer as part of the base.

- 3.5.5 The appellant argued that the problem addressed by the application was to provide an improved method of manufacturing a bipolar junction transistor. Document D3 was not concerned with silicon carbide. Moreover, in document D3 the doped well region was not provided at the bottom of a trench between two pillars and thus not bound on one side. As indicated in the description, the precision with which the base and emitter regions could be spaced using photolithographic techniques was

limited, which could result in undesirably high base resistance and unwanted base-collector capacitance, both of which reduced the ability of the device to operate at high frequencies (cf original description page 3, lines 3 to 11). The use of silicon carbide and the tight control of the physical dimensions of the device, notably the dimensions of the base and the base-emitter spacing, provided a synergistic effect in making the device capable of operating at higher frequencies. There was no suggestion in D3 to increase the frequency range, so there was no reason to turn to silicon carbide. There was no evidence on file of an emitter or base region consisting of a plurality of pillars being known to the skilled person. Document D1 did not concern silicon carbide and provided a different structure with the collector on top. Document D2, disclosed a bipolar junction transistor of silicon carbide, however, without a trench. Thus, starting from document D3, or D2, the skilled person would not arrive at the invention.

3.5.6 However, as discussed above, document D3 concerns bipolar transistors for high-frequency applications. As there is a constant demand for higher operating frequencies, it would be obvious to the skilled person to attempt to further increase the operating frequency. It would thereby be obvious, as discussed above, to turn to silicon carbide and to an interdigitated emitter-base geometry. Moreover, interdigitation with self-aligned base regions inherently leads to the width of the base regions and the base-emitter spacing being tightly controlled, precluding undesirably high base resistance and unwanted base-collector capacitance. It is also noted that no synergistic effect is apparent in

the use of silicon carbide and the tight control of the physical dimensions of the device. Rather, both measures contribute to higher operating frequencies, but the overall effect does not exceed the sum of the technical effects of each measure.

3.5.7 The subject-matter of claim 1, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

Accordingly, the appellant's first auxiliary request is not allowable either.

4. *Second auxiliary request*

4.1 *Amendments*

Claim 1 as amended according to the second auxiliary request is in essence based on claims 1, 10 and 11 as originally filed and on the description as originally filed, page 8, lines 16 to 30 and figures 2 and 3 for the formation of the cap layer, and on page 8, line 8, page 10, lines 6 to 7 and figures 10 and 14 for the definition of the base and emitter regions.

Dependent claim 2 is based on originally filed claim 8. Dependent claims 3 to 5 are based on originally filed claims 5 to 7, respectively. Dependent claim 6 is based on originally filed claim 9. Dependent claim 7 is based on the description as originally filed, page 9, lines 7 to 8.

Independent claim 8 is based on claim 21 as originally filed and on the description as originally filed, page 10, lines 20 to 25 disclosing that the distance

between the pillar and the doped well region is equal to the thickness of the spacer layer and page 9, lines 7 to 8, disclosing a spacer layer thickness of between 0.05 and 0.5 μm .

Accordingly, the amendments comply with Article 123(2) EPC.

4.2 *Article 84 EPC 1973*

Moreover, claim 1 of the second auxiliary request contains the essential features of the invention, in particular those discussed above with respect to claim 1 of the main request, so that the requirements of Article 84 EPC 1973 are considered to be met.

The requirements of Article 84 EPC 1973 are also considered to be met by claim 8, directed at a corresponding bipolar junction transistor, as well as by the remaining dependent claims.

4.3 *Novelty*

Claim 1 of the second auxiliary request, compared to that of the first auxiliary request, only covers the first alternative, in which the first layer (6) and the second layer (8) form a base region and the well region (20) forms an emitter region (ie the first embodiment provided in the description; figures 1 to 10 and 14).

As is apparent from the discussion above of documents D1 to D4, in none of these documents a respective first layer and a pillar formed from a second layer form a

base region and a well region formed in the first layer forms an emitter region.

Accordingly, the subject-matter of claim 1 is new over documents D1 to D4 (Article 54(1) EPC 1973).

For in substance the same reasons above, the subject-matter of independent claim 8, directed at a corresponding bipolar junction transistor fabricated in silicon carbide, is new over documents D1 to D4 (Article 54(1) EPC 1973).

Claims 2 to 7 are dependent on claim 1, providing further limitations. The subject-matter of these claims, therefore, is also new over documents D1 to D4.

4.4 *Inventive step*

As discussed above, in document D3 the pillar formed from the (second) layer (6) of semiconductor material forms an emitter region. The (first) layer (4) of semiconductor material with the doped well region (7) formed therein forms a base region of the transistor. Essentially the same arrangement is provided in document D4. In document D1, pillars form a collector, with adjacent doped well regions forming a base region. In document, D2 in a first embodiment a pillar forms an emitter region (cf figure 2). In another embodiment, a doped well region forms an emitter region (cf figure 3). In this case, however, as discussed above, no adjacent pillar formed from a semiconductor layer forming a base region is provided.

There is nothing in the available prior art suggesting a pillar formed from a layer of silicon carbide (or other semiconductor material) with a doped well region adjacent the pillar forming an emitter region.

Accordingly, having regard to the available state of the art, the subject-matter of claims 1 and 8 is not obvious to a person skilled in the art and, thus, involves an inventive step in the sense of Article 56 EPC 1973.

Claims 2 to 7 are dependent on claim 1, providing further limitations. The subject-matter of these claims, therefore, also involves an inventive step.

5. The patent application documents according to the second auxiliary request also meet the remaining requirements of the EPC, so that a patent can be granted on the basis of these documents.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the following documents:
 - Claims: 1 to 8 according to the second auxiliary request filed during oral proceedings of 19 March 2013;
 - Description pages: 1, 8 to 11, as published; 2 to 7 and 12 to 13, filed during oral proceedings of 19 March 2013;
 - Drawing sheets: 1/8 to 8/8 as published.

Registrar:

Chair:

S. Sánchez Chiquero

G. Eliasson