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Case Number: T 2288/09 - 3.4.03

Application Number: 05768275.9

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Title of invention:
COLUMN AMPLIFIER WITH AUTOMATIC GAIN SELECTION FOR CMOS IMAGE SENSORS

Applicant:
Altasens, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56
EPC Art. 123(2)

Keyword:

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Catchword:

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Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 2288/09 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 23 September 2014

Appellant: (Applicant)	Altasens, Inc. 501 Marin Street 200 Thousand Oaks CA 91360 (US)
Representative:	Lawrence, John Barker Brettell LLP 100 Hagley Road Edgbaston Birmingham B16 8QQ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 7 July 2009 refusing European patent application No. 05768275.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman G. Eliasson
Members: S. Ward
P. Mühlens

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 05 768 275 on the ground that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC.

II. The following documents cited by the Examining Division are referred to in this decision:

D1: US 2002/134918 A1
D3: US 2004/080637 A1
D4: US 6 486 808 B1

III. In the statement of grounds of appeal the appellant requested that the decision be set aside and that a patent be granted on the basis of a main request with claims "in the form refused by the Examining Division" (i.e. claims 1-8 filed with the letter dated 22 September 2008 and claims 9-15 filed with the letter of 9 April 2009), or on the basis of an auxiliary request filed with the statement. With a letter dated 20 August 2014 the appellant filed a second auxiliary request and asked the Board "to consider the enclosed requests in order."

Accompanying the statement of grounds of appeal were "affidavits from two people skilled in the art of CMOS imaging in support of the patentability of the invention."

IV. Oral proceedings before the Board were held in the absence of the appellant, the appellant having previously stated in writing that "the applicant will

not be represented at the oral proceedings scheduled for 23 September 2014."

V. Claim 1 of the main request (including the feature references introduced by the Examining Division in section II.2 of the Reasons) reads as follows:

(a) A column buffer for use in a CMOS image sensor having a plurality of pixels, the column buffer (32) comprising:

(b) an amplifier (52; 62) having an input arranged to receive at least one pixel signal (Vpixel) from a column bus;
the column buffer being characterised by

(c) a comparator (54; 64) for setting a gain level of the amplifier comprising:

(c1) a first input connected to a reference voltage (Vref; Vref2);

(c2, c21) a second input connected to a signal output of the amplifier (52; 62); and

(c3) an output coupled to the amplifier (52; 62), for outputting a comparison result based on the signal levels present at the first and second inputs;

(c4) wherein the gain of the amplifier is first set to a first gain level when the comparison result indicates that the signal output of the amplifier is below the reference signal, such that the amplifier is caused to output a signal amplified according to the first gain level, and

(c5) wherein the gain of the amplifier is set to a second gain level if the comparison result indicates that the signal output of the amplifier is above the reference voltage, such that the amplifier is caused to output a signal amplified according to the second gain level.

Claim 1 of the first auxiliary request differs from claim 1 of the main request in that the following final phrase is inserted:

"and wherein the first gain level is a high-gain level and the second gain level is a low-gain level."

Claim 1 of the second auxiliary request reads as follows:

1. A column buffer for use in a CMOS image sensor having a plurality of pixels, the column buffer (32) comprising:
an amplifier (52; 62) having an input arranged to receive at least one pixel signal (Vpixel) from a column bus;
the column buffer being characterised by
a comparator (54; 64) for setting a gain level of the amplifier comprising:
a first input connected to a reference voltage (Vref; Vref2);
a second input connected to a signal output of the amplifier (52; 62); and
an output coupled to the amplifier (52; 62), for outputting a comparison result based on the signal levels present at the first and second inputs;
wherein the gain of the amplifier is first set to a first gain level, and if the comparison result indicates that the signal output of the amplifier is

below the reference signal the amplifier is caused to output a signal amplified according to the first gain level, otherwise, if the comparison result indicates that the signal output of the amplifier is above the reference voltage, the gain of the amplifier is reduced to a second gain level such that the amplifier is caused to output a signal amplified according to the second gain level, wherein the first gain level is a high-gain level and the second gain level is a low-gain level.

VI. The Examining Division found essentially as follows:

Document D1 was the closest prior art. Novelty over D1 could be acknowledged on the grounds that "although the provision of a comparator and its coupling to the amplifier's output and control input(s) is considered to be at least implicitly disclosed by D1, one cannot safely conclude that the amplifier and the comparator are 'connected' directly as required by claim 1", and furthermore, "the claim can be interpreted as defining an (*sic*) column buffer which integrates both the amplifier and the comparator somehow in one circuit, such as in an integrated circuit, whereas one cannot say that D1 discloses an integration of any kind."

However, "taking account of the obvious design options of a skilled person such distinctions cannot justify an inventive step. This is because firstly, for signal coupling a direct connection is a straightforward solution, and secondly, a skilled person would routinely attempt to modularize resp. integrate circuit components as required to meet obvious design requirements as to size, cost, reliability etc. to arrive at integration of the amplifier and the

comparator of D1 without exercise of an inventive step."

The subject-matter of claim 1 was also considered to be obvious based on the disclosure of document D4.

VII. The appellant argued essentially as follows:

There is no implicit disclosure in D1 of a comparator, nor would it be obvious to a skilled person to provide one. "Paragraph [0047] of D1 states that the signals Gsel1, Gsel2 might be provided 'manually or automatically from outside the system'. This means that these signals could be provided by any one of a number of other systems or arrangements."

The gain of the amplifier in D1 was not set by means of a comparator. As explained in D1 in paragraphs [0094] and [0095], the gain of the amplifier was initially set low, and then increased if the signal output from the amplifier was below the lower limit of the encoding range of the ADC. The obvious way of setting the gain of the amplifier was therefore to simply look at whether the ADC was receiving a signal at all - if it was, the gain of the amplifier must be correct. If it was not, the gain needed to be higher. There was thus no need for a comparator at all, as evidenced by the fact that the inventor of D1 did not suggest it.

Even if, for some non-obvious reason, a skilled person were to decide to use a comparator to control the gain of the amplifier of D1, "means would have to be provided to generate a reference voltage representing the maximum input level of the ADC stage, to serve as one of the inputs to such comparator", and no such means was disclosed in D1 or elsewhere.

Also, if a comparator were used in D1, the output would need to be supplied to whatever entity is supplying signals Gsel1 and Gsel2, so that that entity could decide whether or not to apply signal Gsel1 or signal Gsel2. Supplying the output directly to the amplifier, as claimed, would require re-engineering the way the amplifier of D1 works. It would not be obvious to the skilled man to do this.

Document D4 related to X-ray imaging and was therefore in a different technical field to that of the present invention. D4 was not a document that would be consulted by a person skilled in the art of CMOS imaging. A skilled person would not understand that the controller 20 of D4 was a comparator.

In relation to the first auxiliary request, claim 1 required that the gain be set first to the first (high) gain level. This was precisely the opposite of what is done in D1, in which the gain was initially set to a low level, and then increased if the signal was too small to be detected by the ADC. This began from the assumption that amplification was bad, and should be avoided if possible, whereas the applicant started from the opposite view: "amplify the signal by default, and only reduce the gain of the amplifier if the signal is saturated."

Amplifying the initial analog signals by a factor A at an early stage in the signal processing allowed a corresponding amplification reduction factor of 1/A to be applied at a later stage in processing. This meant noise introduced into the signal by later processing stages could be reduced by a factor of 1/A when

correcting the amplified signals. None of the prior art had appreciated this.

The claims of the second auxiliary request had been amended to more clearly define the differences discussed above with respect to the first auxiliary request. In particular, the gain level was first set to a high gain level, and then reduced to a low gain level.

Reasons for the Decision

1. Main Request

1.1 Both the Examining Division and the appellant based their analyses of inventive step on document D1 as closest prior art; the Board sees no reason to differ.

It is undisputed that document D1 discloses the features (a) and (b) referred to above.

In relation to feature (c), the only comparator explicitly disclosed in document D1 (in paragraphs [0008], [0012] and [0068]) is part of the ADC arrangement and is not concerned with setting the gain of the amplifier. Hence, document D1 does not explicitly disclose a comparator as defined in claim 1 of the main request. The question is therefore whether such a comparator is *implicitly* disclosed.

The manner in which the gain of the amplifier is adjusted in document D1 is set out in general terms in paragraph [0047] as follows:

"*if a difference signal outputted from the operational amplifier 31 is out of a range of a digital encoding analog input level to the column type ADC 106 of a next stage, an amplifying gain needs to be adjusted to set the difference signal within the range of the analog input level. Accordingly, signals (Gsel1 and Gsel2) are supplied manually or automatically from the outside in order to select at least one of the fifth and sixth switch devices SW5 and SW6 to control ON/OFF thereof.*"

This passage does not specify precisely how it is determined whether the amplifier output signal is or is not "out of a range of a digital encoding analog input level". It is also somewhat vague on the manner in which the gain control signals (Gsel1 and Gsel2) are generated ("manually or automatically from outside the system"). However, clarification is provided further on in the description by the explanation that a "difference signal" Vs is derived from the output of the operational amplifier 31 (paragraph [0093]), and that:

"*the difference signal Vs* ***is compared with*** *the range of the digital encoding analog input level.*" (Paragraph [0094], emphasis added by the Board.)

In the same paragraph it is further explained that:

"If a level of the difference signal Vs is within the range of the digital encoding analog input level, the difference signal is directly outputted to the column type ADC 106."

If this is not the case, the consequence is described in paragraph [0095]:

"*On the other hand, when the level of the difference signal Vs is smaller than, for example a lower limit of the range of the digital encoding analog input level, a capacitance of the feedback capacitor Cf is selected based on a signal from outside such that the difference signal Vs is amplified by a gain so as to set the level of the difference signal Vs larger than the lower limit.*"

Hence, document D1 unequivocally discloses that the gain of the amplifier is set based on the result of a *comparison of two voltages*, namely a reference voltage (a "lower limit of the range of the digital encoding analog input level") and a signal output of the amplifier (Vs). However, the means by which this comparison is made is not explicitly disclosed.

The term "comparator" does not denote a generic device for comparing two voltages, but refers to a specific type of device which compares two input analogue voltages and outputs a digital signal indicating which is larger. A comparator is not the *only* device or arrangement capable of comparing two voltages, and hence the comparison of voltages referred to above does not necessarily imply the use of a comparator, since other means of performing this operation are conceivable. Consequently, feature (c) of claim 1 is not considered to be implicitly disclosed in document D1.

Document D1 does, however, disclose the claimed features (c4) and (c5), in that the gain of the amplifier is first set to a first (higher) gain level when the comparison result indicates that the signal output of the amplifier is below the reference signal,

such that the amplifier is caused to output a signal (Vsamp) amplified according to the first gain level, and the gain of the amplifier is set to a second gain level (unity) if the comparison result indicates that the signal output of the amplifier is above the reference voltage, such that the amplifier is caused to output a signal (Vs) amplified according to the second gain level (paragraphs [0094]-[0097]).

The subject-matter of claim 1 of the main request therefore differs from document D1 in defining a comparator (feature (c)) and the manner in which the comparator is connected (features (c1)-(c3)).

1.2 The problem solved by this distinguishing feature can only be seen as providing a practical implementation of the voltage comparison disclosed in document D1.

Even if the use of a comparator is not implicit in document D1, comparators are very well known circuit elements which are routinely employed to compare two analog voltages to determine which is greater, and hence the use of a comparator would represent an obvious possibility to the skilled person, especially as the voltage comparison which is performed in the subsequent circuit module (ADC 106) is explicitly disclosed as being performed by a comparator (paragraphs [0008], [0012] and [0068]). Hence no inventive step can be seen in feature (c).

Moreover, the skilled person would have no difficulty in implementing such a measure. Clearly the analog inputs to the comparator must be the two voltages disclosed as being compared, namely a reference voltage corresponding to the lower limit of the range of encoding of the ADC and a signal output of the

amplifier (Vs). The output (i.e. the comparison result) would be coupled to the amplifier to control the capacitance of feedback capacitor Cf as mentioned in paragraph [0095] thereby controlling the gain. Hence the skilled person would also arrive in an obvious manner at features (c1)-(c3) of claim 1 of the main request.

1.3 The arguments of the appellant and the (similar) arguments presented in the two affidavits do not persuade the Board.

The Board does not agree that there is no feedback loop disclosed in document Dl. According to document D1 the gain of the amplifier is set based on the result of a comparison of two voltages, one of which is the difference signal Vs derived from the output of the amplifier, hence a feedback loop is implicit.

The appellant's suggestion that the the obvious way of setting the gain of the amplifier would be "to simply look at whether the ADC is receiving a signal at all" is beside the point. The procedure for setting the gain of the amplifier is *disclosed* in document D1 and does not correspond to this suggestion. Instead, as explained above, the gain level is set on the basis of a comparison of a signal output of the amplifier (Vs) with a lower limit of the range of digital encoding. Only the means for making the comparison is not disclosed.

Even if no means is explicitly disclosed in document Dl to generate a reference voltage "to serve as one of the inputs to such comparator", since document D1 discloses comparing the signal Vs and the analog lower voltage limit for digital encoding, it is clear that *whatever*

means is chosen to make the comparison, these two voltages would have to be supplied to the comparison means to enable them to be compared.

The Board concurs with the appellant that "if a comparator were used in D1, the output would need to be supplied to whatever entity is supplying signals Gsel1 and Gsel2, so that that entity could decide whether or not to apply signal Gsel1 or signal Gsel2." Indeed, whether or not a comparator were used to arrive at the disclosed comparison result, some such control arrangement is implicit.

The appellant concludes that this distinguishes the invention over the prior art since supplying "the output directly to the amplifier, as claimed" is not disclosed in document D1, a point also raised by the Examining Division. However, in claim 1 the comparator output is merely defined to be "coupled" to the amplifier, which does not necessarily imply a direct connection. In fact, according to the arrangements disclosed in the present application, the output from the comparator is not directly connected to the amplifier, but to a switching arrangement, shown schematically in figure 6, which controls the amplifier gain by selectively connecting capacitors C1-C4.

Moreover, although the Board agrees with the Examining Division that it would be obvious, for the reasons outlined above, to connect a signal output of the amplifier (Vs) *directly* to the input of the comparator, it is not in fact essential to the development of the argument to establish this, as claim 1 merely defines them to be "connected" (hence, directly or indirectly).

It is furthermore not necessary for the Board to decide whether the column buffer of the present application represents a more "integrated" arrangement than that of document D1, as this does not correspond to any feature of claim 1.

In the light of the above, the Board concludes that the subject-matter of claim 1 of the main request does not involve an inventive step within the meaning of Article 56 EPC 1973.

2. First Auxiliary Request

2.1 In addition to the features of claim 1 of the main request, claim 1 of the first auxiliary request defines that the first gain level (when the signal output of the amplifier is below the reference signal) is a high gain level and the second gain level (when the signal output of the amplifier is above the reference signal) is a low-gain level.

The appellant argues that whereas in document D1 the gain of the amplifier is initially set to a low level, according to claim 1 of the first auxiliary request, the gain is first set to a high gain level, as defined by the following feature:

"the gain of the amplifier is first set to a first gain level when the comparison result indicates that the signal output of the amplifier is below the reference signal ...".

The appellant apparently interprets this feature as defining a number of separate steps: the gain of the amplifier is first set to a first gain level *prior to* the voltage comparison, the voltage comparison is

made, and finally the gain is set again to a high or low level depending on the comparison result.

The Board's view is that such an interpretation reads features into the claim which are simply not there. Although the wording is not entirely unambiguous, the Board sees no justification for interpreting this feature as defining some form of gain initialization prior to the voltage comparison. What is defined is that the gain of the amplifier is set at a first (high) gain level "when" the result of the comparison is known – hence *after* the comparison has been made – provided the result indicates that the amplifier output is below the reference signal, otherwise the gain is set to the second (low) gain level.

In this formulation, therefore, the words "first" and "second" are merely labels distinguishing the two gain levels (high and low) which may be set after the determination of the comparison result. Whether the gain of the amplifier *prior* to the determination of the comparison result is set at the first gain level, the second gain level or some other gain level is not defined.

As explained above, according to paragraphs [0094] and [0095] of document D1, if Vs is below a reference voltage - a lower limit of the range of the digital encoding analog input level - Vs is amplified with a certain gain (which may be referred to as a first or high gain level). When Vs is within the range (i.e. above the lower limit) the signal is directly sent to the column type ADC 106, i.e. the gain is set to the lower level of unity (which may be referred to as a second or low gain level). The additional feature is therefore disclosed in document D1, and hence the

subject-matter of claim 1 of the first auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973.

2.2 The Board furthermore wishes to point out that as neither claim 1 of the main request nor claim 1 of the first auxiliary request are considered to define the gain of the amplifier *prior* to the determination of the comparison result, it may be doubted whether the claimed subject-matter complies with the requirements of Article 123(2) EPC. Nevertheless, as the Board finds neither of these requests allowable based on the ground which led to refusal (lack of inventive step), it is not considered necessary to pursue this matter further.

3. Second Auxiliary Request

3.1 Claim 1 of the second auxiliary request, which was filed after the Board's provisional opinion had been issued, specifies that:

"the gain of the amplifier is first set to a first gain level, and if the comparison result indicates that the signal output of the amplifier is below the reference signal the amplifier is caused to output a signal amplified according to the first gain level, otherwise, if the comparison result indicates that the signal output of the amplifier is above the reference voltage, the gain of the amplifier is reduced to a second gain level such that the amplifier is caused to output a signal amplified according to the second gain level, wherein the first gain level is a high-gain level and the second gain level is a low-gain level."

The Board's understanding of this feature is that (implicitly for each readout procedure) the gain level

of the amplifier is initialized to a high level *prior* to the determination of the comparison result; thereafter the comparator compares the signal output of the amplifier with the reference voltage and sets the amplifier gain accordingly (high or low), and readout is performed at this gain level. Thus, the feature of initializing the gain to a high level, which the appellant sought to read into claim 1 of the first auxiliary request, has been satisfactorily defined in claim 1 of the second auxiliary request.

3.2 The appellant argues that "D1 does not disclose setting the gain of the amplifier first to a high level and then reducing it to a low level" (emphasis in the original), but "setting the gain low and only increasing it if the signal is too low to be detected".

By contrast, the appellant "starts from the opposite view: amplify the signal by default, and only reduce the gain of the amplifier if the signal is saturated", since "amplifying the signal as a standard - rather than only as a last resort - has the beneficial effect that the noise contribution of subsequent processing stages can be reduced." Furthermore, the "cited prior art has not appreciated this advantage".

Terms such as "default" or "standard" in relation to the gain or amplification are not used in the application, but the Board understands these terms, as used by the appellant, to refer to the gain which is intended to be employed in the majority of readout cycles, a different gain being used only by way of exception.

Clearly the "default" gain depends on the level at which the reference voltage is set. In document D1 the

reference voltage is set at a low level, namely the lower level at which the ADC can operate. Generally signal outputs will be above this level and will therefore experience a "default" low gain (unity); only the signal outputs which are below this lower threshold (presumably a minority) will experience a high gain.

By contrast, according to the description of the present application, the reference voltage is set at a high level, such that only column buffer output signals which would exceed the system's dynamic range will exceed the reference voltage, and for these signals a low or unity gain is set (see page 6, lines 6-17). All signal outputs below the reference voltage will experience a high gain - referred to by the appellant as the "default" amplification - and a consequent improvement in noise performance (page 5, lines 15-22).

While the appellant's observations on these differences are not wrong *per se*, they are nevertheless not convincing, as the appellant is effectively arguing for the grant of a European patent based on features which, although present in the description, are not present in the sole independent claim.

In particular, there is no feature in claim 1 of the second auxiliary request indicating "amplifying the signal as a standard" or that high gain is the "default". Furthermore, no particular level is claimed for the reference voltage (which determines the "default" gain, as as explained above). Claim 1 of the second auxiliary request therefore includes embodiments in which the reference voltage is set, as in document D1, at the lower level at which the ADC can operate, and hence in which the default gain is low or unity.

For such embodiments no technical advantage in initializing the gain to a high level can be seen. On the contrary, such a measure would appear to lead to the disadvantage that in most readout cycles the initialized high gain would not be the same as the gain determined by the comparison result, and hence additional switching operations would be required which would not occur in the arrangement of document D1.

In a number of decisions the boards of appeal have held that subject-matter does not involve an inventive step if it involves a modification of the closest prior art which is predictably disadvantageous and where the disadvantage is not compensated by any unexpected technical advantage (Case Law of the Boards of Appeal, 7th edition 2013, I.D.9.18.1). Hence, no inventive step can be seen in the subject-matter of claim 1 of the second auxiliary request.

3.3 The Board wishes to remark in passing that it does not accept the appellant's position that the prior art does not furnish any examples of programmable gain control with high default gain to reduce noise while avoiding saturation. This approach is disclosed in document D3 (paragraphs [0065]-[0066]), and document D4 also teaches the use of "the maximum possible output signal voltage without device or circuit saturation" (column 3, lines 58-60).

Also as an aside, it is noted that according to claim 1 of the second auxiliary request the gain level actually set (and implicitly used for data readout) is that determined by the comparison result. The Board does not find any convincing explanation why – even in the case of a high default gain – the gain level prior to this determination is significant.

These points need not be pursued in the present decision, however, as the Board is satisfied, for the reasons already set out above, that the subject-matter of claim 1 of the second auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated