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**Datasheet for the decision
of 18 March 2014**

Case Number: T 0731/10 - 3.2.02

Application Number: 98952096.0

Publication Number: 1019117

IPC: A61M1/12, G06F19/00

Language of the proceedings: EN

Title of invention:

Controller module for implantable pump system

Patent Proprietor:

Micromed Technology, Inc.

Opponent:

STRAWMAN LIMITED

Headword:

Relevant legal provisions:

EPC Art. 54, 56

Keyword:

Novelty - (yes)
Inventive step - (yes)

Decisions cited:

Catchword:



**Beschwerdekammern
Boards of Appeal
Chambres de recours**

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0731/10 - 3.2.02

**D E C I S I O N
of Technical Board of Appeal 3.2.02
of 18 March 2014**

Appellant: STRAWMAN LIMITED
(Opponent) 34 Lovedon Lane
Winchester,
Hampshire, SO23 7NU (GB)

Representative: DeVile, Jonathan Mark
D Young & Co LLP
120 Holborn
London EC1N 2DY (GB)

Respondent: Micromed Technology, Inc.
(Patent Proprietor) 1610 Woodstead Court,
Suite 360
The Woodlands,
Texas 77380 (US)

Representative: Mounteney, Simon James
Marks & Clerk LLP
90 Long Acre
London
WC2E 9RA (GB)

Decision under appeal: **Interlocutory decision of the Opposition
Division of the European Patent Office posted on
8 February 2010 concerning maintenance of the
European Patent No. 1019117 in amended form.**

Composition of the Board:

Chairman: E. Dufrasne
Members: C. Körber
D. Ceccarelli

Summary of Facts and Submissions

- I. On 8 February 2010 the Opposition Division posted its interlocutory decision concerning maintenance of European patent No. 1019117 in amended form.
- II. An appeal was lodged against this decision by the opponent by notice received on 7 April 2010. The appeal fee was paid on 31 March 2010. The statement setting out the grounds of appeal was received on 7 June 2010.
- III. By communication of 3 January 2014, the Board forwarded its provisional opinion to the parties and summoned them to oral proceedings.
- IV. With letters dated 27 February 2014 and 12 March 2014, respectively, the appellant (opponent) and the respondent (patent proprietor) both indicated that they would not attend the oral proceedings.
- V. Oral proceedings were held on 18 March 2014 in the absence of the parties in accordance with Rule 115(2) EPC and Article 15(3) RPBA.

The requests of the parties were as follows:

The appellant had requested in writing that the decision under appeal be set aside and that the patent be revoked in its entirety.

The respondent had requested in writing that the appeal be dismissed.

- VI. The following documents are of importance for the present decision:

D2: CA 2 161 383

D3a: English translation of JP 9-225022.

VII. Claim 1 of the patent as accepted for maintenance by the Opposition Division reads as follows (with the feature denotation given in the annex attached to the statement of grounds of appeal being indicated at the left margin):

1. "A controller module (16) for an implantable pump system including a pump (12) having an electric motor (38), the controller module (16) comprising:
 - 1.1 a processor (80),
 - 1.2 a motor controller (84) electrically coupled to the processor (80),
 - 1.2.1 the motor controller (84) connectable to an implantable pump system motor
 - 1.2.2 and operable to power a pump motor (38) connected thereto such that the pump motor (38) operates at a desired speed,
 - 1.2.3 the motor controller (84) adapted to receive operating parameter information from the pump motor (38) connected thereto
 - 1.2.4 and output digital representations of the pump motor operating parameters to the processor (80),
 - 1.3 a first memory device (122) coupled to the processor (80)
 - 1.3.1 for storing the digital data representing system operating parameters, and
 - 1.4 a user interface (126) coupled to the processor (80)
 - 1.4.1 for displaying the pump motor operating parameters,
 - 1.5 wherein the first memory device (122) comprises a plurality of memory banks (SRAM0, SRAM1, SRAM2),
 - 1.6 wherein the processor (80) is programmed such that at least one of the memory banks is operated as a circular buffer

- 1.6.1 for continuously storing real-time pump motor parameters in predefined time increments, and
- 1.7 the plurality of memory banks (SRAM0, SRAM1, SRAM2) comprises at least first and second memory banks (SRAM0, SRAM1),
- 1.8 wherein the processor (80) is programmed to operate the circular buffer in the memory on the first memory bank (SRAM0), and
- 1.9 wherein the processor (80) is programmed to transfer the data from the first memory bank (SRAM0) to the second memory bank (SRAM1) upon a first predetermined event, characterised in that
- 1.10 the plurality of memory (SRAM0, SRAM1, SRAM2) further comprises a third memory bank (SRAM2),
- 1.11 wherein the processor (80) is programmed to transfer the data from the first memory bank (SRAM0) to the third memory bank (SRAM2) upon any predetermined events subsequent to the first predetermined event."

Claims 2 to 9 are dependent claims.

VIII. The appellant's arguments are summarised as follows:

Document D3a anticipated feature 1.11 of claim 1. The three memory banks defined in claim 1 were formed by the two internal memories (82, 84) and the memory card (70) of D3a. The transfer of data from the first memory bank to the second memory bank upon a first predetermined event was disclosed in paragraph [0053], where it was stated that past driving status data was transferred to the memory card (70) when the memory card was reinserted. If the memory card was then inserted for a second time, data was transferred again from the internal memories (82, 84) to the memory card (70). In this respect the memory card acted as both the

second and the third memory bank, thus anticipating feature 1.11. Removing and reinserting the memory card (70) was undeniably a predetermined event. Claim 1 did not limit what was considered to be a predetermined event. The effect on the processor of D3a when the memory card (70) was removed and reinserted was effectively the same as that of a pump fail/restart in the patent in suit: both events corresponded to an emergency situation where data needed to be preserved. This was the essence of what was meant by "predetermined event" in the alleged invention. Removing/reinserting the memory card (70) was thus a subsequent predetermined event in precisely the same way as was a pump fail/restart in the patent in suit. The only question therefore that remained regarding the novelty of claim 1 was whether the memory card (70) so removed and reinserted could form the third memory bank. However, because claim 1 did not limit the definition of the third memory bank in any way, the only way to assess what was meant by the third memory was to look at its function. From paragraph [0055] of the specification of the patent in suit it became clear that the function of the third memory was to always contain the data associated with the most recent event. In exactly the same way, the memory card (70) of D3a was intended to always contain the data associated with the most recent event, as it was at this point that data was transferred to it (upon reinsertion). This interpretation was in no way illogical. On the contrary, the predetermined event had exactly the same characteristic as in the alleged invention (the triggering of the preservation of data) and the third memory bank also served the same purpose (to contain the most recent information). Accordingly, the disclosure of D3a read onto the subject-matter of claim 1.

The technical effect of feature 1.11 was to preserve the data which had been transferred after the initial predetermined event, but to keep all data after subsequent events in a different memory bank. Thus, so long as the data in the first memory bank was preserved, the data in the third memory bank could be overwritten. Thus, the problem was actually related to data logging. In view of the technical effect, the objective technical problem could be considered to be the provision of a controller module which could always store the first and last set of data. When starting from D3a and considering how to store two sets of data independently, the skilled person would use the common general knowledge that RAM based PC cards typically contain different segments of memory which the processor would write to. Thus, upon noting that the initial data kept being overwritten every time the memory card was reinserted, the skilled person would simply use a PC card with discrete segments of memory and program the processor to write to these segments following reinsertion of the card. It was quite obvious that where two sets of data needed to be stored and where the first always remained the same and the second always changed, the second set could be constantly overwritten, but the first must not be. Any skilled person in the field of data logging understood this. As soon as it was set out that the first set of data was fixed and the last set of data constantly updated, the only logical way to arrange the processor and memory was to ensure that the first set of data and the last set of data were stored in different segments of memory. Accordingly, the subject-matter of claim 1 was obvious from D3a and the common general knowledge.

D2 provided a disclosure of data logging in the field of biomedical instruments with a recorder which included a circular buffer and a memory device such that occurrences of distinct events triggered a transfer of data from the circular buffer to the memory device. This document would thus be taken into consideration by the skilled person when starting from D3a. D2 disclosed an arrangement in which data was transferred from a circular buffer into memory following a first event and from the circular buffer into memory following a subsequent event, so that the data for each of these events could be analysed. The only difference between a combination of D3a and D2 was the explicit recitation of a separate memory for storing data for a subsequent event, because in D2 the data from the circular buffer for two events was transferred into the same memory, whereas according to claim 1 the data was transferred into separate memory banks. However, the choice of using one large memory or two separate memories could not confer an inventive step because this represented a mere design selection. Moreover a virtual memory was typically comprised of more than one physical memory bank, and so the provision of separate memory banks could be regarded as implicit. A separation of the memory into three banks was somewhat arbitrary and did not confer any technical effect.

Page 2, line 24, to page 3, line 2, of D2 explicitly related to the problem in the art of data acquisition and logging where previous systems had overwritten data related to an earlier event when recording later data. Thus, previous systems had not had the ability to preserve initial data, whilst still being able to record later data. D2 explicitly stated that whereas prior art devices had destroyed the initial data, the invention of D2 transferred data to a separate memory

device and only overwrote that data with data relating to another occurrence of the same distinct event. This was the critical teaching in D2 which led the skilled person to the subject-matter of claim 1. D2 envisaged the problem of overwriting data from one type of event with data from another type of event. In order to avoid this problem, D2 taught that data was overwritten only where there was another occurrence of the same distinct event, i.e. that data from the first predetermined event could be overwritten only by data from other "first predetermined events". Given that there would only ever be one first predetermined event, the data in the first memory bank would never be overwritten. In contrast, where data was collected from many subsequent predetermined events, i.e. the last predetermined event, the previously collected data for this event would be overwritten. The data related to the first predetermined event were transferred to a memory bank and never overwritten (because there was never another occurrence of the "first predetermined event"). The data related to any subsequent predetermined events were transferred to a further memory bank and overwritten "upon another occurrence" of such a subsequent event. In this way D2 provided the solution of claim 1. The respondent's argument that D2 taught to create a plurality of data logs in a single memory bank, rather than a plurality of memory banks within a single memory device, was an artificial one. Claim 1 did not place any limitation on what could be considered to be a "memory bank", and the depiction of the first memory device (122) in Figure 3 of the patent in suit did not show that each segment was a discrete and distinct memory bank.

- IX. The respondent's arguments are in essence those on which the following reasons of this decision are based.

Reasons for the Decision

1. The appeal is admissible.
2. Novelty

The appellant regards the features of the characterising portion of claim 1 as being anticipated by document D3a, with the two internal memories (82, 84) and the memory card (70) constituting the three memory banks as defined in features 1.7 and 1.10 of claim 1. Even if this interpretation is followed, the Board does not share the appellant's respective conclusions for the following reasons. If the memory card is inserted (constituting a "first predetermined event" as referred to in feature 1.9), it is stated in paragraph [0053] of D3a that data are transferred from the internal memories (82 and 84) to the memory card (70). Accordingly, the memory card (70) may be regarded as acting as the second memory bank, thus anticipating feature 1.9 of claim 1. However, the Board does not accept the appellant's argument that, upon removal and reinsertion of the card (constituting a predetermined event subsequent to the first predetermined event), the memory card (70) at that time acts as a third memory bank as defined in the characterising portion of claim 1. The claim wording makes a clear distinction between the second and the third memory bank, denoted as SRAM1 and SRAM2 respectively. In Figure 3, the respective segments are shown as discrete and distinct elements (in contrast to what is stated by the appellant). Accordingly, these memory banks form separate entities, and the memory card (70) of D3a cannot be said to constitute both the second and the third memory bank. There is nothing in the disclosure of D3a that would

support such an interpretation. Since D3a fails to disclose (at least) feature 1.11 of claim 1, its subject-matter is novel within the meaning of Article 54 EPC.

3. Inventive step

3.1 According to feature 1.11, data representing system operation parameters obtained for all predetermined events subsequent to the first predetermined event are stored in the third memory bank. The technical effect resulting therefrom is that data of the first predetermined event are held by their own by having been stored separately in the second memory bank, where they cannot be overwritten by the data relating to the predetermined events subsequent to the first predetermined event. In contrast, the data on the memory card (70) of D3a, including those relating to the first predetermined event, are continuously overwritten in a ring buffer fashion as explained in paragraph [0052]. The first occurrence of a predetermined event is likely to be significant, and therefore it is highly desirable to preserve data relating to that first predetermined event. As disclosed in paragraphs [0054] and [0055] of the specification of the patent in suit, the first predetermined event may be a pump shutdown and restart, which is highly significant and potentially dangerous to the patient. Therefore it is very important for a physician or a technician to obtain and assess pump motor information relating to that first predetermined event. Analysis of such information may not be possible immediately once the first predetermined event has occurred. Therefore, according to claim 1, this information is preserved by storing it in the second memory bank and by separating the data obtained for all

subsequent predetermined events into a different, third memory bank.

- 3.2 The objective technical problem is thus to provide a controller module that keeps important data representing system operating parameters of the implantable pump relating to a first predetermined event available for later access and analysis.
- 3.3 In D3a itself, this problem is nowhere addressed, and there is nothing in this document which suggests the solution as provided by claim 1 to the skilled person. The Board does not share the appellant's view that the skilled person, when starting from D3a and considering how to keep data relating to a first predetermined event while saving data relating to any subsequent predetermined event, would use the common general knowledge that RAM based PC cards typically contain different segments of memory which the processor would write to. This approach already contains a pointer to the claimed solution, which resides in storing two sets of data independently. It is also not agreed that the only logical way to arrange the processor and memory is to ensure that the first set of data and the last set of data are stored in different segments of memory as soon as it is set out that the first set of data is fixed and the last set of data constantly updated. This view is based on hindsight. Accordingly, the subject-matter of claim 1 is not obvious from D3a and the common general knowledge.
- 3.4 The fact that D2 relates to event history data acquisition does not imply that the skilled person starting from D3a would not consider its teachings at all, as suggested by the respondent. D2 provides a general disclosure of data logging in a recorder which

includes a circular buffer and a memory device such that occurrences of distinct events trigger a transfer of data from the circular buffer to the memory device. As disclosed on page 1 of D2, such data recording technology is known to be applied in the field of electrocardiograph (EKG) and electroencephalograph (EEG) machines, blood pressure meters and other biomedical instruments. The Board is thus of the opinion that the skilled person starting from D3a would indeed consider the teachings of D2.

In D2, for a distinct event type there are two alternatives presented, as detailed in lines 13 to 25 of its page 15. In the first alternative, the data log transferred from the circular buffer to a memory device will contain data elements relating to the most recent occurrence of the distinct event, to replace any existing data log therein. Accordingly, the data elements are susceptible of being overwritten and thus not inescapably preserved for later access.

In the second alternative in D2, the data log formed when a distinct event initially occurs is retained, and a new data log is formed in the same memory device for each subsequent occurrence of such a distinct event. However, in lines 23 to 25 of page 15 it is also mentioned that in case of insufficient storage capacity within the memory device the data logs are updated in the order in which they were formed. Accordingly, these data logs are also susceptible of being overwritten and thus not inescapably preserved for later access.

Also in the passage cited by the appellant on page 2, line 24, to page 2a, line 2, of D2 it is mentioned that the data relating to a distinct event "is not destroyed **unless it is overwritten by data relating to another**

occurrence of the same event" [emphasis added], i.e. it **is** susceptible of being overwritten. The Board cannot follow the appellant's argument that there will only ever be one first predetermined event and that the data will hence never be overwritten.

There is no teaching or suggestion in D2 of storing particularly important data relating to the occurrence of a first predetermined event separately and securely, in a different memory bank, without being susceptible of being overwritten by data relating to any predetermined events occurring subsequent to the first predetermined event.

The appellant also argued that the only difference of claim 1 over a combination of D3a and D2 was the explicit recitation of a separate memory for storing data for a subsequent event. In view of the technical effect thereby achieved as indicated above, this cannot be regarded as "a mere design selection".

Accordingly, the subject-matter of claim 1 is also not obvious from D3a in combination with D2.

3.5 In conclusion, the subject-matter of claim 1 is based on an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



D. Hampe

E. Dufrasne

Decision electronically authenticated