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Datasheet for the decision of 17 July 2014

Case Number: T 0918/10 - 3.4.03

Application Number: 01923120.8

Publication Number: 1309993

IPC: H01L21/768

Language of the proceedings: EN

Title of invention:
COPPER INTERCONNECTS WITH IMPROVED ELECTROMIGRATION RESISTANCE AND LOW RESISTIVITY

Applicant:
ADVANCED MICRO DEVICES, INC.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - (no) all requests - obvious alternative

Decisions cited:
T 0602/03

Catchword:

This datasheet is not part of the Decision.
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Case Number: T 0918/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 17 July 2014

Appellant: (Applicant)	ADVANCED MICRO DEVICES, INC. One AMD Place Mail Stop 68 P.O. Box 3453 Sunnyvale CA 94088-3453 (US)
Representative:	Brookes Batchellor LLP 46 Chancery Lane London WC2A 1JE (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 7 October 2009 refusing European patent application No. 01923120.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	V. L. P. Frank
Members:	T. M. Häusser
	P. Mühlens

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division refusing the European patent application No. 01 923 120 for lack of inventive step (Article 56 EPC 1973).

II. The appellant requested in writing that the decision of the examining division be set aside and a patent be granted on the basis of the main request, the first auxiliary request or the second auxiliary request, all filed with the letter dated 17 June 2014.

III. The oral proceedings before the board were held in the absence of the appellant, of which the board had been informed with the letter dated 23 June 2014.

IV. Reference is made to the following documents:

D1: EP 0 877 421 A2,
D3: EP 0 856 884 A2.

V. The wording of independent claim 4 of the main request and the respective independent claim 3 of the first and second auxiliary requests is as follows:

Main request:

"4. A semiconductor device (200), comprising:
a plurality of levels of dielectric layers and conductive layers formed on a semiconductor substrate (20); and
an interconnect formed in at least one of the dielectric layers,
the interconnect electrically connecting at least two of the conductive layers or one of the conductive

layers and an active region in the semiconductor substrate (20),

the interconnect being characterized by:

a layer of doped copper (50) formed along a bottom (42) and sidewalls (40) of the interconnect;

a lower portion comprising substantially pure copper (30), the substantially pure copper (30) being encapsulated in the lower portion of the interconnect by the layer of doped copper (50) formed along the bottom (42) and sidewalls (40), and

an upper portion comprising doped copper (32)."

First auxiliary request:

Independent claim 3 of the first auxiliary request differs from independent claim 4 of the main request in comprising the following additional features:

"wherein a thickness of the layer of doped copper is between 20nm and 100nm, and
the layer of doped copper deposited along the bottom and sidewalls of the opening contains from about 0.3% to about 12% by weight of a dopant element".

Second auxiliary request:

Independent claim 3 of the second auxiliary request is identical with independent claim 4 of the main request.

VI. The appellant argues essentially as follows in relation to inventive step:

Document D1 disclosed that the copper alloy layer 100 might be deposited cold in a sputter process, but during the deposition of the pure copper layer 102 or afterwards in a separate annealing step the temperature

was raised sufficiently high to cause the alloying element of the copper alloy to migrate to the dielectric layer 64. It was further disclosed that the copper alloy layer 100 might be deposited with the wafer held at an elevated temperature.

In contrast, document D3 was directed to a method for providing improved via fill in high aspect ratio apertures at low temperature. In particular, the chemical vapour deposition (CVD) Cu layer was deposited onto the refractory layer at low temperatures and the physical vapour deposition (PVD) Cu layer was deposited onto the previously formed CVD Cu layer at a temperature below that of the melting point temperature of Cu.

Furthermore, document D1 did not disclose depositing another copper layer over the pure copper layer 102.

In view of these differences it could not be seen how the substitution of the thin tantalum layer 16 of D3 with the copper alloy layer of D1 would not have an effect on the purpose of D3 to provide improved via fill in high aspect ratio apertures at low temperature and to obtain a CVD Cu / PVD Cu layer that was essentially void-free. Furthermore, in view of the temperature differences a skilled person would not be led to combine these documents.

Additionally, in document D3 it was disclosed that the PVD Cu layer might contain certain dopants and that upon deposition the PVD Cu might integrate with the CVD Cu so that the dopant was dispersed throughout much of the CVD Cu / PVD Cu intermetallic layer 24. However, this increased the resistivity of the interconnect, which in turn was leading to slower processing

associated with the semiconductor device. Hence, the skilled person would not look to document D3 to overcome the deficiencies in document D1.

The invention was concerned with the technical problem of improving low electromigration problems associated with copper interconnects while maintaining low resistivity of the interconnect. This was solved by the claimed subject-matter.

Therefore, the subject-matter of claim 4 of the main request involved an inventive step over document D3 in combination with document D1.

Furthermore, these arguments should also to be considered in relation to the first and second auxiliary requests.

Reasons for the Decision

1. The appeal is admissible.

2. Procedural matters

2.1 Claim 4 of the main request and claim 3 of the first and second auxiliary request, respectively, were submitted in response to the summons to oral proceedings before the board. The duly summoned appellant was not represented at the oral proceedings. The proceedings were however continued without the appellant in accordance with Rule 71(2) EPC 1973. In view of Article 113(1) EPC 1973, the board had to consider whether it was in a position to decide on these claims.

2.2 According to Article 15(3) RPBA, the board "shall not be obliged to delay any step in the proceedings, including its decision, by reason only of the absence at the oral proceedings of any party duly summoned who may then be treated as relying only on its written case". The purpose of oral proceedings is to give the party the opportunity to present its case and to be heard. However, a party gives up that opportunity if it does not attend the oral proceedings.

2.3 It is established case law of the boards of appeal that an appellant who submits amended claims shortly before the oral proceedings and subsequently does not attend these proceedings must expect a decision based on objections which might arise against such claims in his absence (see e.g. T 602/03, point 7 of the Reasons).

Therefore, an appellant who submits new claims after oral proceedings have been arranged but does not attend these proceedings must expect that the board decides that the new claims are not allowable because of deficiencies, such as for example lack of inventive step.

2.4 In the present case, claim 4 of the main request and claim 3 of the first and second auxiliary requests, respectively, were found to lack inventive step as detailed below.

The appellant had to expect a discussion during oral proceedings on inventive step of the subject-matter of its newly filed claims, in particular because the board had made the preliminary remark in the communication under Article 15(1) RPBA that this issue would be discussed at the oral proceedings.

Furthermore, claim 4 of the main request and claim 3 of the second auxiliary request are identical with claim 4 previously on file. In the above communication the board had stated its preliminary opinion that the subject-matter of this previous claim lacked inventive step over document D3 in combination with document D1.

Moreover, claim 3 of the first auxiliary request comprised the features of claim 4 previously on file and two additional features taken from the description. However, in the letter submitted in response to the summons to oral proceedings before the board the appellant had provided no arguments how these additional features taken from the description added to the presence of inventive step of the subject-matter of claim 3 of the first auxiliary request.

2.5 Due to the appellant's absence in the oral proceedings, relevant issues regarding inventive step could not be discussed with the appellant. However, a duly summoned appellant who by his own volition does not attend the oral proceedings cannot be in a more advantageous position than he would have been in if he had attended.

The voluntary absence of the appellant can therefore not be a reason for the board not to raise issues it would have raised if the appellant had been present. Since the appellant did not appear in order to explain why the subject-matter of the claims involved an inventive step, the board could only rely on the appellant's written submissions. The voluntary absence of the appellant was not a reason for delaying a decision and the board was also in a position to decide at the conclusion of the oral proceedings, since the case was ready for decision (Article 15(5) and (6) RPBA).

3. Main request - inventive step

3.1 Closest state of the art

Document D3 is conceived for the same purpose as the claimed invention, namely for providing a semiconductor device with a plurality of dielectric layers and conductive layers and an interconnect formed in one of the dielectric layers. Furthermore, document D3 has the most relevant technical features in common with the claimed invention as detailed below. Document D3 is therefore regarded as the closest state of the art.

3.2 Distinguishing features

3.2.1 In particular, document D3 relates to (see page 3, lines 3-5; page 5, lines 6-19; page 6, lines 38-53; claim 17; Figures 1 and 2) a metallization process for manufacturing semiconductor devices and wafers, in particular to the metallization of apertures to form void-free interconnections between conducting layers. A substrate has a patterned dielectric layer 12 having a via 14 formed thereon. A thin tantalum layer 16 is directly deposited onto the substrate covering substantially all surfaces of the dielectric layer 12 including the walls 18 and floor 20 of the via 14. A conformal chemical vapour deposition (CVD) Cu layer 22 is deposited on the tantalum layer 16 to a desired thickness. Furthermore, a physical vapour deposition (PVD) Cu layer 23, which may contain certain dopants such as tin, is deposited onto the CVD Cu layer 22. The tantalum layer 16 provides greater wetting with the CVD Cu than does the dielectric and prevents the diffusion of copper into the adjacent dielectric material.

3.2.2 Using the wording of claim 4 of the main request, document D3 discloses a semiconductor device, comprising:
a plurality of levels of dielectric layers and conductive layers formed on a semiconductor substrate (wafer, conducting layers, dielectric layer); and an interconnect (via 14) formed in at least one of the dielectric layers (dielectric layer 12), the interconnect (via 14) electrically connecting at least two of the conductive layers (interconnection between conducting layers), the interconnect (via 14) comprising:
an encapsulating layer (tantalum layer 16) formed along a bottom and side-walls of the interconnect (tantalum layer 16 covering substantially all surfaces of the dielectric layer 12 including the walls 18 and floor 20 of the via 14), a lower portion comprising substantially pure copper (CVD Cu layer 22), the substantially pure copper being encapsulated in the lower portion of the interconnect (via 14) by the encapsulating layer (tantalum layer 16) formed along the bottom (floor 20) and side-walls (walls 18), and an upper portion comprising doped copper (PVD Cu layer 23 containing dopant such as tin).

Therefore, the subject-matter of claim 4 of the main request differs from the device of document D3 in that:
(i) the encapsulating layer is a doped copper layer.

3.3 Objective technical problem

3.3.1 The appellant is of the opinion that the invention was concerned with the technical problem of improving electromigration problems associated with copper interconnects while maintaining low resistivity of the interconnect.

This is the *subjective* technical problem as originally presented in the application as filed (see the description of the application, page 2, lines 13-15).

However, the subjective technical problem may need to be reformulated in view of prior art documents which are more relevant than those which had originally been taken into account by the applicant when drafting the application as filed. The relevant factor in determining the objectively solved problem is the effect actually achieved in relation to the closest state of the art.

Therefore, in the present case it has to be assessed what the effect is of using a doped copper layer as an encapsulating layer as opposed to the tantalum layer used in the closest state of the art.

3.3.2 The purpose of using the doped copper layer in the claimed invention is to improve electromigration resistance of the interconnect, thereby improving the reliability of the semiconductor device (see the description of the application, page 5, lines 39-41).

In document D3 it is described that the tantalum layer is necessary to prevent diffusion of copper into the adjacent dielectric material which can cause electric shorts to occur (D3, page 5, lines 13-14).

The doped copper layer and the tantalum layer are therefore considered to serve the *same purpose* of providing a barrier layer preventing copper atoms to diffuse into the dielectric, thus preventing shorts and improving the reliability of the device.

Therefore, the *objective* technical problem is to provide an alternative barrier layer.

3.4 Obviousness

3.4.1 The skilled person, a semiconductor physicist, would consider document D1, which relates to metal deposition in the fabrication of semiconductor integrated circuits.

Document D1 discloses in relation to the embodiment shown in Figure 10 (see D1, abstract; page 7, line 7 - page 8, line 1, Figure 10; also page 4, line 55 - page 5, line 6, Figure 5) a copper-based interconnect or pad 62 formed in the surface of a lower dielectric layer 60. An upper level dielectric layer 64 is deposited over the lower dielectric layer 60 and a via hole 66 is etched through the upper dielectric layer 64 in the area of the copper pad 62. A conformal copper alloy film 100 is deposited into the via hole 66 and on top of the second dielectric layer 64. In a separate deposition process the copper layer 102 is deposited filling the via hole 66 and overlying the upper dielectric layer 64. The alloying percentages will range up to 10 atomic %, but Mg alloying should be kept below 6 atomic % and Al alloying should be kept below 0.3 atomic % (page 7, lines 55-58). The purpose of the copper alloy film is to act both as a wetting layer and as a barrier layer preventing copper from diffusing into and through the second dielectric layer 64 (page 7, lines 15-23; see also page 9, lines 14-16).

3.4.2 The appellant is of the opinion that in document D1 a high temperature was used during deposition of the copper alloy layer or during a subsequent annealing

step, whereas low temperatures were used in the method of D3.

In document D1 the temperature of the sputtering and annealing is described as "elevated" or "high". In detail however, it is described in relation to the embodiment mentioned above that the sputtering of the copper alloy is performed at room temperature with subsequent annealing at 500°C; alternatively, hot sputtering at a temperature between 200°C and 400°C is used (D1, page 7, lines 7-54). In document D3 it is described that the invention provided improved via fill in high aspect ratio apertures at "low temperature". In particular, it is described that the CVD Cu layer 22 and the PVD Cu layer 23 are both deposited at temperatures below about 400°C (D3, page 6, paragraphs 1 and 2). Even though different words are used to describe the temperatures in documents D1 and D3, the copper and copper alloy layers are in fact deposited at similar temperatures in both documents. The skilled person would therefore not be discouraged to replace the tantalum layer in the device of document D3 by the copper alloy layer of document D1. Rather, he would be led to use for the deposition of the copper alloy layer in the device of D3 a temperature that is similar to the temperatures already used for the deposition of the CVD Cu layer 22 and the PVD Cu layer 23.

3.4.3 The appellant further argues that document D1 did not disclose depositing another copper layer over the pure copper layer 102. In view of this and the temperature differences it could not be seen how the substitution of the tantalum layer with the copper alloy layer would not have an effect on the purpose of D3 to provide void-free vias.

Document D3 cites a study of CVD Al layers formed on substrates indicating that the formation of voids occurs through a key hole process wherein the top portion of the via becomes sealed before the via has been entirely filled. Continued CVD deposition to complete filling of vias typically results in the formation of voids therein. On the other hand, hot PVD Al processes are very sensitive to the quality of the wetting layer, wafer condition and other processing parameters. Small variations in processing conditions and/or poor coverage of the wetting layer could result in incomplete filling of the contacts or vias, thus creating voids. In order to overcome these problems and to achieve void-free layers, document D3 proposes to form a thin refractory barrier/wetting layer on the substrate followed by a thin conformal CVD Cu layer; a PVD CU layer is then deposited over the CVD Cu layer (D3, page 3, line 22 - page 4, line 37).

Document D1 also cites the problem of creating voids when filling high-aspect ratio holes with metal for the interlevel connection. Two techniques to overcome the problem were mentioned: directional sputtering and reflow. It was further stated that directional sputtering is not required by the invention according to D1, but advantageously used in conjunction with it (D1, page 3, line 38 - page 4, line 3). In relation to the embodiment of Figure 10 mentioned above it is furthermore stated that the copper layer 102 readily fills the via hole coated with the copper alloy film 100 so the second copper deposition does not require special hole filling techniques (D1, page 7, lines 20-22). It is thus evident that it is not even necessary to use directional sputtering to avoid the creation of voids.

Replacing the tantalum layer 16 in the device of document D3 by the copper alloy layer of document D1 would therefore still allow the vias to be filled void-free.

3.4.4 In view of the low concentrations (less than 6 or 0.3 atomic % for Mg, respectively Al) of the alloying element, the copper alloy layer may be considered as a doped copper layer within the meaning of that expression in claim 4 of the main request, especially as that layer is also referred to as a "copper alloy seed layer" in the description of the application (see page 5, lines 18-24).

3.4.5 In view of the above the board considers that it would be obvious for the skilled person to replace the tantalum layer 16 in the device of document D3 by a doped copper layer in order to provide an alternative barrier layer.

Therefore, the subject-matter of claim 4 of the main request does not involve an inventive step, contrary to the corresponding requirement of Article 52(1) EPC in combination with Article 56 EPC 1973.

4. First auxiliary request - inventive step

4.1 Closest state of the art / distinguishing features

Independent claim 3 of the first auxiliary request differs from independent claim 4 of the main request in comprising the following additional features:

(ii) wherein a thickness of the layer of doped copper is between 20nm and 100nm, and

(iii) the layer of doped copper deposited along the bottom and sidewalls of the opening contains from about 0.3% to about 12% by weight of a dopant element.

The subject-matter of claim 3 of the first auxiliary request differs therefore from document D3, which is still regarded to represent the closest state of the art, in comprising features (i), (ii) and (iii).

4.2 Objective technical problem

Concerning feature (ii) it is stated in the description of the application (see page 5, lines 25-26) that the thickness of the layer of doped copper may be in the claimed range "depending on the particular circuit requirements". Furthermore, in relation to feature (iii) it is stated that the percentage by weight of the dopant element in the layer of doped copper may be in the claimed range "based on the particular dopant and the particular circuit requirements".

The objective technical problem is therefore to provide an alternative barrier layer in a manner that is compatible with the particular dopant and the particular circuit requirements.

4.3 Obviousness

In the description of the application it is stated that the present invention has particular applicability to high density semiconductor devices with submicron design features (page 1, lines 4-6). Similarly,

document D3 relates to contacts of vias in high aspect ratio sub-half micron applications (D3, page 3, lines 3-5).

Furthermore, in the description of the application it is mentioned that - among others - magnesium and aluminium may be used as the dopant element for the layer of doped copper (page 5, lines 27-28). Both of these elements are also mentioned as dopant elements in document D1 (see D1, page 7, line 55 - page 8, line 1).

The circuit requirements and the requirements in relation to the dopant concentration are therefore similar in the present invention and in the documents D1 and D3.

Correspondingly, it is explicitly mentioned in document D1 in relation to the embodiment mentioned above that the Mg should be kept below 6 atomic % in the copper alloy. In view of the atomic masses of Mg and Cu this value falls within the claimed range of weight percentage of the dopant. Furthermore, in relation to a similar embodiment shown in Figure 11 of D1 it is disclosed that the thickness of the copper alloy layer is preferably no more than 50nm (D1, page 8, lines 21-27) thus also falling within the claimed range.

The board therefore considers that the skilled person would, when replacing the tantalum layer 16 in the device of document D3 by a doped copper layer as indicated above under point 3, choose the thickness of the doped copper layer and the dopant concentration by weight to fall within the claimed respective ranges in order to provide a device that is compatible with the particular dopant and the particular circuit requirements.

Therefore, the subject-matter of claim 3 of the first auxiliary request does not involve an inventive step, contrary to the corresponding requirement of Article 52(1) EPC in combination with Article 56 EPC 1973.

5. Second auxiliary request - inventive step

Claim 3 of the second auxiliary request is identical with claim 4 of the main request, whose subject-matter does not involve an inventive step for the reasons given above under point 3.

Therefore, the subject-matter of claim 3 of the second auxiliary request does not involve an inventive step, either, contrary to the corresponding requirement of Article 52(1) EPC in combination with Article 56 EPC 1973.

6. Conclusion

Since each request comprises at least one claim whose subject-matter does not involve an inventive step, none of the requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero V. L. P. Frank

Decision electronically authenticated