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**Datasheet for the decision
of 26 November 2014**

Case Number: T 1643/10 - 3.5.06

Application Number: 00100018.1

Publication Number: 1022641

IPC: G06F1/04, G06F1/12, G06F13/00,
G06F13/16, G06F13/36,
G06F13/38, G11C7/00, G11C8/00,
G11C8/04

Language of the proceedings: EN

Title of invention:
System containing a plurality of DRAMS and a bus

Patent Proprietor:
Rambus Inc.

Opponents:
SK hynix Deutschland GmbH
(opposition withdrawn)
MICRON EUROPE Ltd
(opposition withdrawn)

Headword:
Bus architecture/RAMBUS

Relevant legal provisions:
EPC 1973 Art. 76(1)
EPC Art. 123(2)

Keyword:
Amendments - deletion of features (yes) -
added subject matter (yes)

Decisions cited:

G 0002/10, T 0331/87, T 0789/89, T 0167/93, T 0081/03,
T 0265/05

Catchword:



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Case Number: T 1643/10 - 3.5.06

**D E C I S I O N
of Technical Board of Appeal 3.5.06
of 26 November 2014**

Appellant:
(Patent Proprietor)

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Decision under appeal:

**Interlocutory decision of the Opposition
Division of the European Patent Office posted on
14 July 2010 concerning maintenance of the
European Patent No. 1022641 in amended form.**

Composition of the Board:

Chairman	W. Sekretaruk
Members:	M. Müller
	A. Teale

Summary of Facts and Submissions

- I. The appeal lies against the interlocutory decision of the opposition division, with reasons dated 14 July 2010, that, account being taken of the amendments made by the patent proprietor during the opposition proceedings, the patent EP B 1022641, in the amended form based on what was then auxiliary request 4, and the invention to which it related met the requirements of the EPC.

- II. The European patent application No. 00100018.1 leading to the patent in suit was filed as a divisional application of European patent application No. 91908374.1 which had originally been filed as International patent application PCT/US91/02590 and been published as WO91/16680. The present application as originally filed contained as part of its description all claims of the International application relabelled as "embodiments" (albeit under the heading "Claims" and the opening phrase "What is claimed is:") and with an amended set of claims 1 to 28. The published version of the present application however lacks claims 1 to 28 as originally filed and only lists as claims what was originally filed as "embodiments".

- III. In the appealed decision the main request and auxiliary requests 1 to 3 were found not to comply with Articles 76(1) and 123(2) EPC (see decision, reasons 7.5) due to the omission of a feature from claim (or "embodiment") 103 which had been presented as essential in the originally filed description of the earlier and the present applications and which thus failed the essentiality test. The feature in question was "said bus containing substantially fewer lines than the number of bits in a single address" which in claim 1 had been replaced by

"the bus uses address multiplexing to convey a single memory address" (decision under appeal, reasons 7.1).

IV. Appeals against this decision were filed by the proprietor and both opponents.

Opponent I, in its grounds of appeal, argued *inter alia* that the decisions T 81/03 and T 265/05, which related, respectively, to the parent application and another of its divisional applications, constituted *res iudicata* for the present case.

Both opponents meanwhile withdrew both their oppositions and appeals. The opponents have thus ceased to be parties to the proceedings except for issues relating to the apportionment of costs (see T 789/89, OJ EPO 1994, 482, headnote) which have not arisen in the present proceedings. The proprietor is thus the only remaining appellant and will be referred to simply as "appellant" below.

The proprietor's notice of appeal was received on 29 July 2010, the appeal fee being paid on the same day. In its statement of grounds of appeal the appellant requested that the appeal be set aside and that the patent be maintained based on claim 1 according to a main request or one of auxiliary requests I to VII as filed with the letter received on 1 March 2011 and the grounds of appeal, respectively. The main request and auxiliary requests I to III correspond to the requests upon which the appealed decision is based, whereas auxiliary request V corresponds to auxiliary request 4, the basis upon which the amended patent was found to comply with the EPC. Auxiliary request IV corresponds to auxiliary request V with the difference

that claim 1 specifies the bus to have "fewer bus lines" rather than "substantially fewer bus lines".

V. In an annex to a summons to oral proceedings the board set out its preliminary opinion that it shared the conclusion of the opposition division that claim 1 of the main request and of auxiliary requests I to III did not comply with Articles 76(1) and 123(2) EPC. With regard to new auxiliary request IV the board noted *inter alia* that the appeal did not address the added subject-matter objection. While the board thus tended to the opinion that the appeal would probably have to be dismissed, it made remarks regarding the further procedure in case the board were to decide on the added matter question in the appellant's favour. In particular, the board noted that, due to the prohibition of *reformatio in peius*, since the proprietor was the only remaining appellant, it could not challenge maintenance of the patent based on auxiliary request V.

VI. In response to the summons, by letter dated 2 October 2014, the appellant withdrew auxiliary requests V to VII but maintained auxiliary requests I to IV and provided arguments in favour of the main request. Primarily it argued that the added subject-matter objection relied on an incorrect interpretation of the omitted feature and that it was, properly construed, equivalent to the feature by which it was replaced. Hence, the scope of the claim did not change due to the the omission of the feature. If the board were to find that the omission had extended the scope of the claim, the appellant argued that the omission should nonetheless be allowed according to the "essentiality test" according to T 331/87 or according to a criterion used in the BGH decision X ZR 107/12 which the board was asked to adopt.

VII. At the oral proceedings on 26 November 2014 the appellant requested that the decision under appeal be set aside and the European patent be maintained on the basis of the main request or one of the auxiliary requests I - IV, all filed with the letter dated 12 November 2010. At the end of the oral proceedings the chairman announced the decision of the board.

VIII. Claim 1 of the main request reads as follows:

"A system comprising:

a bus that includes a plurality of bus lines for carrying substantially all address, data and control information needed by each semiconductor device coupled to the bus for communication with substantially every other semiconductor device connected to the bus, wherein the bus uses address multiplexing to convey a single memory address; and

a plurality of synchronous dynamic random access memory (DRAM) semiconductor devices coupled to the bus, each DRAM of the plurality of synchronous DRAM semiconductor devices including:

connection means adapted to connect the DRAM to the bus;

clock receiver circuitry (101, 111) for receiving a clock signal (53, 54);

a programmable access-time register for storing a value which is representative of a number of clock cycles of the clock signal (53, 54) to transpire after which the DRAM responds to a read request received synchronously with respect to the clock signal, the programmable

access-time register being accessible to the bus through the connection means, wherein data is transmitted to the programmable access-time register over the bus to set the value in the programmable access-time register; and

a plurality of output drivers (76) for outputting data onto the bus (18, 65) in response to the read request, wherein the output drivers (76) output the data on the bus (18, 65) after the number of clock cycles of the clock signal transpire and synchronously with respect to the clock signal (53, 54), so that the read request and the corresponding response are separated by the number of clock cycles as selected by the value stored in the programmable access-time register, wherein each output driver of the plurality of output drivers (76) outputs the data onto the bus (18,65) at a bus cycle data rate that is twice the rate of the clock signal."

IX. Claim 1 of auxiliary request I differs from claim 1 of the main request only in that the "clock signal" is qualified to be an "external clock signal".

X. Claim 1 of auxiliary request II is the same as claim 1 of auxiliary request I from the beginning to the expression "external clock signal;" and from thereon, reads as follows:

"a programmable access-time register for storing a value which is representative of a read access-time and a write access-time, the programmable access-time register being accessible to the bus through the connection means, wherein data is transmitted to the programmable access-time register over the bus to set the value in the programmable access-time register;

a plurality of output drivers (76) for outputting read data onto the bus (18, 65) in response to a read request received synchronously with respect to the external clock signal, wherein the output drivers (76) output the read data on the bus (18, 65) after a number of clock cycles of the external clock signal corresponding to the read access-time transpires and synchronously with respect to the external clock signal (53, 54), so that the read request and the corresponding response to the read request are separated by the number of clock cycles corresponding to the read access-time, wherein each output driver of the plurality of output drivers (76) outputs the read data onto the bus (18, 65) at a bus cycle data rate that is twice the rate of the external clock signal; and

a plurality of input receivers for inputting write data from the bus in response to a write request received synchronously with respect to the external clock signal, wherein the input receivers input the write data from the bus after a number of clock cycles of the external clock signal corresponding to the write access-time transpires and synchronously with respect to the external clock signal, so that the write request and the corresponding response to the write request are separated by the number of clock cycles corresponding to the write access-time."

- XI. Claim 1 of auxiliary request III is the same as claim 1 of auxiliary request II except that the following feature has been added at the end:

"and a plurality of sense amplifiers to receive the write data to be stored in an array in the memory device and to sense the read data, wherein the read

request includes precharge information indicating whether to precharge the sense amplifiers after sensing the read data, and wherein the write request includes precharge information indicating whether to precharge the sense amplifiers after storing the write data in the array."

- XII. Claim 1 of auxiliary request IV corresponds to claim 1 of auxiliary request I except that at the end of the initial bus feature (see lines 2 to 6) the following phrase has been inserted:

"and wherein the bus has fewer bus lines than the number of bits in a single address".

- XIII. The earlier application as originally filed contained, *inter alia*, the following claims 103 and 104:

"103. A semiconductor device capable of use in a semiconductor bus architecture including a plurality of semiconductor devices connected in parallel to a bus wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to said bus, and has substantially fewer bus lines than the number of bits in a single address, said semiconductor device comprising

connection means adapted to connect said semiconductor device to said bus, and

at least one modifiable access-time register accessible to said bus through said connection means, whereby data may be transmitted to said register via said bus which establishes a predetermined amount of

time that said semiconductor device thereafter must wait before using said bus in response to a request.

104. The semiconductor device of claim 103 wherein said semiconductor device is a memory device which connects substantially only to said bus and sends and receives substantially all address, data and control information over said bus."

XIV. The precise wording of originally filed claims 1-28 is immaterial for the present decision.

Reasons for the Decision

1. Res iudicata

1.1 It was argued by former opponent I that earlier decisions T 81/03 and T 265/05 constituted *res iudicata* (as defined in T 167/93, reasons 2.5; OJ EPO 1997, 229) for the present case and that the board was correspondingly barred from dealing with issues upon which the earlier decision had already decided.

1.2 As a matter of law, the board must assess this issue of its own motion even though both oppositions were withdrawn.

1.3 In both T 81/03 and T 265/05 the board decided on claims comprising the feature of a "bus [which] has substantially fewer lines than the number of bits in a single address" and found Article 123(2) EPC to be complied with (see T 81/03, facts X and reasons 3.10, and T 265/05, facts X and reasons 1.5). Thus neither of them contains any final decision regarding the question

of whether a claim lacking that feature conforms to Articles 76(1) EPC 1973 or 123(2) EPC.

1.4 Hence, at least with respect to this question, the decisions cannot constitute *res iudicata* for the present appeal. As the appeal is decided on just that question, it may be left open whether or to what extent decisions regarding a parent or a cibling application represent *res iudicata* for a divisional application at all.

2. Main request and auxiliary requests I-III

2.1 It is to be decided whether claim 1 according to the main request or auxiliary requests I-III conforms to Articles 76(1) EPC 1973 and 123(2) EPC even though they do not specify the feature that the "bus has substantially fewer bus lines than the number of bits in a single address". This feature defines a relationship between the bus width and the address width but does not imply anything about the absolute size of either (as the appellant correctly points out, see letter of 2 October 2014, p. 2, point II.1). This notwithstanding and for the sake of brevity only, this feature will be referred to below as the requirement of a "narrow bus".

2.2 The proprietor argues that claim 1 according to all requests is based on embodiment 103 of the application as originally filed for the purpose of Article 123(2) - and, for the purpose of Article 76(1) EPC 1973, of claim 103 of the parent application as originally filed. In the following both will, for simplicity, be jointly referred to as "claim 103".

2.3 The preamble of claim 103 specifies a "semiconductor device capable of use in a semiconductor bus archi-

- tecture including a plurality of semiconductor devices connected in parallel to a bus ...".
- 2.4 The board notes that, literally, the claimed "semiconductor device" and the "plurality of semiconductor devices" which constitute the "semiconductor bus architecture" are different from and need not be related to each other. Thus any limitation that the claimed bus may have on the "plurality of semiconductor devices" need not automatically imply a corresponding limitation of the claimed semiconductor device.
- 2.5 This observation notwithstanding, the board considers that the skilled person would indeed take as implicit that the claimed semiconductor device is one of those (or at least of the same type as those) constituting the semiconductor bus architecture and that, consequently, limitations of the latter do imply limitations of the former.
- 2.6 To the extent that the semiconductor devices are only claimed to be "capable of use" in the claimed architecture, they need only be "capable of [being] connected" to the claimed "narrow" bus.
- 2.7 The board agrees with the appellant that the "capab[ility] of [being] connected" to a narrow bus implies the capability of multiplexing (large addresses on few bus lines). The board also accepts the appellant's position that a semiconductor device which can be connected to a narrow bus can also be connected to a wider bus, e.g. by leaving any additional bus lines unused.
- 2.8 However, claim 103 also specifies a "connection means adapted to connect said semiconductor device to said bus". Regardless of whether the claimed semiconductor

- device is one of or of the same type as the "plurality of semiconductor devices", this means that the semiconductor device must be *adapted for connection* with the narrow bus mentioned in original claim 103.
- 2.9 As disclosed in original claims (or "embodiments") 82 and 92, the connecting means consists of pins for connection to the external bus and corresponding wires for connection with the internal bus logic.
- 2.10 The adaptation of the semiconductor device for connection with the narrow bus does not limit the number of pins the semiconductor device has, as there may be unused pins just as there may be unused bus lines. However, the number of pins carrying bus signals is determined by the internal bus logic.
- 2.11 Therefore, the "narrow bus" feature in combination with the connecting means adapted to it implies that the claimed semiconductor device "has substantially fewer" pins carrying bus signals "than the number of bits in a single address".
- 2.12 Claim 1 of the main request implies that the claimed semiconductor device performs "address multiplexing to convey a single memory address". This implies that the number of address lines used to transmit a single address is smaller than the address width. How much smaller is, strictly speaking, not implied, since addresses must be multiplexed on the bus even if the addresses are only one bit wider than the bus. However, the board considers that the skilled person would understand address multiplexing to imply that there are "substantially fewer" bus lines than address bits. This corresponds to the general observation that, for optimal usage of the limited bus resource, the address

width should be a multiple of the bus width, but also to the specific disclosure that "very large addresses" (such as 40 bits wide) "can be sent over a small number of bus lines" (such as 8) or that an address may be split into row and column addresses which can be transmitted over a "bus only half as wide" (see application as filed, p. 2, last para. to p. 3, 1st para.; fig. 1; and p. 12, lines 5 to 10).

2.13 However, the bus is defined to carry "substantially all address, data and control information". Neither claim 1 of the main request nor original claim 103 specifies whether addresses, data and control information are to be sent over the same or different bus lines or whether the connecting means has separate pins for each.

2.14 The requirement that the semiconductor device support address multiplexing may imply a limitation of the number of address pins of the semiconductor device but does not imply such a limitation on the number of data and control pins. Accordingly, the semiconductor device according to claim 1 of the main request may connect to a bus which has few address lines but an unspecified number of data and control lines, so that the entire bus to which it is adapted to connect need not be substantially narrower than the address width but may, in fact, be wider.

2.15 The appellant argued that claim 103 did not exclude further pins beyond those needed for the bus, for instance if the semiconductor device had to be connected to a second bus as depicted in figure 9. The board agrees. However, such additional pins - irrespective of their intended purpose - do not affect the limitation which claim 103 sets out on the pins constituting the connection means which is specified to be "adapted to

- connect said semiconductor device to said bus" as claimed.
- 2.16 The board therefore comes to the conclusion that the replacement of the "narrow bus" feature by the address multiplexing feature broadens the scope of the claim and constitutes the omission of a feature of claim 103. This conclusion applies to claim 1 of the main request and auxiliary requests I to III.
- 2.17 It thus needs to be decided whether the omission of the "narrow bus" feature is in conformance with Articles 76(1) EPC 1973 and 123(2) EPC.
- 2.18 Article 123(2) EPC provides that a European patent application may not be amended in such a way that it contains subject-matter which extends beyond the content of the application as filed, and Article 76(1) EPC 1973 provides that a divisional application may be filed only in respect of subject-matter which does not extend beyond the content of the earlier application as filed.
- 2.19 The appellant argues that omission of the "narrow bus" feature was justified, if exceptionally, because for the skilled person the size of the bus relative to the address width was apparently not part of the actual invention.
- 2.20 The appellant observes that address multiplexing to allow for the use of smaller buses was well-established at the priority date of the present application and disclosed as such (see the background section regarding fig. 1). It was therefore clear, in fact and from the application as filed, that the relative bus width did not constitute the invention (see e.g. letter of 2 Oc-

tober 2014, p. 19, 2nd para.). Rather, the actual invention according to claim 103 was the provision of the programmable access-time register which made the response of the memory chip predictable and thus allowed a more effective use of the available bus - which had to be treated as a limited resource (see that letter, p. 14, last para. ff.).

2.21 The appellant argued (see letter of 2 October 2014, p. 12 ff., point 6) that the German Federal Court of Justice (Bundesgerichtshof BGH) in its decision X ZR 107/12, whilst applying the same fundamental legal prohibition of added subject-matter as the EPO, put weight on the skilled person's appreciation ("Wertung") as to which features had to be attributed to the "real invention" (die "eigentliche Erfindung") and allowed the omission of those features which did not contribute to the solution of the problem as apparent from the original application documents. According to this standard, which the appellant considered to be more permissive than the usual practice at the EPO and which it suggested that the board adopt, the omission of the "narrow bus" feature should be allowed as evidently not a part of the actual invention. Alternatively, the appellant argued that omission of that feature should be allowed according to the "essentiality test" of T 331/87 (headnote; OJ EPO 1991, 22) because it was neither essential for the actual invention nor, in particular, disclosed as being an essential feature of the invention in the application as originally filed (see that letter, p. 22, item iv).

2.22 The enlarged board of appeal has, in several decisions, established that under Article 123(2) EPC an amendment is only allowable within the limits of what a skilled person would derive directly and unambiguously, using

common general knowledge, and seen objectively and relative to the date of filing, from the application as originally filed (see e.g. G 2/10, reasons 4.3; OJ EPO 2012, 376). The board is not convinced that the BGH decision discloses a substantially different standard, but this question need not be decided because the board sees no compelling reason to question the criterion established by the enlarged board of appeal.

2.23 Apart from technical facts and necessities, an application contains an exposition of what the applicant at the time of filing considered to be the invention. This exposition may present a feature as a part of the invention even though that feature may, in fact, not be necessary for achieving a central effect of invention. The applicant's understanding of which feature is part of the invention may change after the filing date in view of new technical insight as to which features are necessary to achieve the desired effect or in view of a new understanding as to which effect of the claimed invention is actually important for the appellant. The applicant may also come to the opinion that the originally filed application does not say precisely what it was intended to say. Later insights such as these cannot be invoked to justify an amendment which otherwise goes beyond the application as originally filed. Thus the content of the application as originally filed comprises - and is hence also limited by - what the applicant decided to disclose as forming part of the invention at the time of filing.

2.24 In the present case, the board notes that the "narrow bus" feature was not only contained in claim 103 but, in fact, in all but two independent claims of the earlier application, namely claims 1, 13, 25, 46, 56, 68, 82, 97, 103, 106, 108, 111, 114, 116, 118, 121, 124 and

135. The only exceptions are claims 73 and 91 which however relate to the clocking of a "bus subsystem" and a "package" comprising a "semiconductor die", respectively, irrespective of how many lines the pertinent bus contains. Neither claim 73 nor claim 91 however refers to the address width either, so that they need not - and, in fact, cannot reasonably - make any statement about the relative bus width. Also claims 1-28 as originally filed in the present application imply nothing on the relative address and bus widths. Hence, all original independent claims of the earlier application and all corresponding "embodiments" - and in fact, original claims - of the present application which mention an address width at all also specify - and thus disclose - that the bus is substantially narrower than the address width. Moreover, again in the present application and the earlier, also the section entitled "summary of the invention" mentions this feature.

2.25 On page 8, lines 4 to 7, as originally filed it is disclosed that "16 bus lines or other numbers of bus lines can be used". The appellant takes this to disclose that the bus may have an essentially arbitrary number of lines and specifically to disclose a bus which is not substantially narrower than the address width. The board considers that the skilled person would not have read this passage as suggested by the appellant. This passage does not exclude a narrow bus because a bus may be narrow but still not be limited to a fixed number of lines. The passage, therefore, does not disclose, directly and unambiguously, that the number of bus lines may be anything other than "substantially fewer than" the address width. The board therefore concludes that the cited paragraph cannot justify the omission of the narrow bus feature.

- 2.26 Figure 9 illustrates the possibility that a semiconductor device may be connected to more than one bus. As already stated however, this implies that the semiconductor device may have more pins than needed for one bus but allows no conclusion to be reached as to the number and meaning of the pins connecting to one bus as claimed.
- 2.27 Also the other passages of the description referred to by the appellant, especially page 6 (2nd para.) to page 7 (1st para.), page 12 (1st para.) and page 42 (last para.) do not support the appellant's case. These passages all relate to the goal of allowing the use of a small bus and of reducing the pin count of the semiconductor device accordingly, but do not disclose a semiconductor device which connects to a bus which is not "substantially" smaller than the address width.
- 2.28 The board therefore comes to the conclusion that the omitted feature was, in fact, disclosed as an integral part of the invention and that the subject-matter of claim 1 of the main request without that feature cannot be derived directly and unambiguously, and seen objectively, from the present application or the earlier application as originally filed. Claim 1 of the main request thus does not comply with Articles 76(1) EPC 1973 and 123(2) EPC. The board is of the opinion that the differences between claim 1 of auxiliary requests I to III and that of the main request do not affect this reasoning, and the appellant did not argue this to be the case either. Therefore, also claim 1 of auxiliary requests I to III does not conform with Articles 76(1) EPC 1973 and 123(2) EPC. This deficiency thus prejudices the maintenance of the patent on the basis of these requests.

3. Auxiliary request IV

3.1 The appellant did not explain in the grounds of appeal (see point IV) why auxiliary request IV was "inserted" between auxiliary requests III and V.

3.2 In the annex to the summons to oral proceedings, the board speculated that the appellant might have filed auxiliary request IV to address the possibility that the board might find auxiliary request 4 as maintained to lack clarity due to the use of the term "substantially", contrary to the decision under appeal (see reasons II). In the presence of two appellant-opponents this was a possible outcome of the appeal proceedings for which the proprietor might have wanted to be prepared. In its letter of 2 October 2014 (sentence bridging pages 1 and 2), the appellant confirmed the board's understanding in this respect.

3.3 Presently, however, since the proprietor is the sole remaining appellant, the patent, in the form found to comply with the EPC by the opposition division, cannot be challenged by the board due to the prohibition of *reformatio in peius*. As a defence against a potential clarity objection to the term "substantially" therefore, auxiliary request IV is not necessary.

3.4 Claim 1 of the auxiliary request IV corresponds to the one which the opposition division found to comply with the EPC with the exception that the bus is only required to have "fewer" - but not necessarily "substantially fewer" - bus lines than the number of bits in an address.

3.5 As "substantially fewer" is a more limiting condition than "fewer" it is observed that the wording of claim 1

of the auxiliary request IV differs from that consistently used throughout the earlier application and the original application as filed (see esp. above point 2.24). *Prima facie* at least this modification therefore constitutes a violation of Articles 76(1) EPC 1973 and 123(2) EPC.

3.6 In its summons to oral proceedings, the board had noted the absence of reasons from the grounds of appeal as to why auxiliary request IV could overcome the main objection in the decision under appeal. The appellant however did not provide any argument as to why the feature that the "bus has fewer bus lines than the number of bits in a single address" did not go beyond the content of the (present and earlier) application as originally filed, neither in writing nor during oral proceedings.

3.7 The board therefore concludes that claim 1 of auxiliary request IV does not comply with Articles 76(1) EPC 1973 and 123(2) EPC.

Summary

4. None of the appellant's requests is allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



B. Atienza Vivancos

W. Sekretaruk

Decision electronically authenticated