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Datasheet for the decision of 18 September 2014

Case Number: T 1682/10 - 3.4.03

Application Number: 99961985.1

Publication Number: 1086496

IPC: H01L29/778, H01L29/24

Language of the proceedings: EN

Title of invention:
NITRIDE BASED TRANSISTORS ON SEMI-INSULATING SILICON CARBIDE SUBSTRATES

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC Art. 123(2)
EPC 1973 Art. 56

Keyword:
Inventive step (no)

Decisions cited:

Catchword:

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Case Number: T 1682/10 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 18 September 2014

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Brophy, David Timothy FRKelly 27 Clyde Road Ballsbridge Dublin 4 (IE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 12 March 2010 refusing European patent application No. 99961985.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	R. Bekkering
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the refusal of application no. 99 961 985 for added subject-matter, Article 123(2) EPC (main request) and for lack of an inventive step, Article 56 EPC (auxiliary request), over documents

D1: Gaska R et al: "*High-Temperature Performance Of AlGaN/GaN HFET's on SiC Substrates*", IEEE Electron Device Letters, US, IEEE Inc New York, vol 18, no 10, 1 October 1997, pages 492 to 494, and

D2: WO 96 24167 A.

II. A summons to oral proceedings was issued by the board, provided with an annex in which a provisional opinion of the board on the matter was given.

In particular, the appellant was informed that it appeared that the appellant's request for reimbursement of the appeal fee by reason of a substantial procedural violation in the first instance proceedings (Rule 103(1)(a) EPC) had to be refused, as no procedural violation was seen to have taken place.

Moreover, the appellant was informed that it appeared that claim 1 of the main request filed with the statement setting out the grounds of appeal had been amended so that it contained subject-matter extending beyond the content of the application as filed, contrary to the requirement of Article 123(2) EPC. Furthermore, claims 3 and 10 lacked clarity, Article 84 EPC 1973.

Moreover, it appeared that the subject-matter of claim

1 of the main request lacked an inventive step in the sense of Article 56 EPC 1973 over documents D1 and D2, as well as over document

D3: US 4 426 656 A.

One or more of these objections also applied to the first to fifth auxiliary request filed with the statement setting out the grounds of appeal.

III. With a letter of reply dated 13 August 2014, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following:

Claims 1 to 10 according to the appellant's main (and only) request, filed with this letter.

With a letter dated 9 September 2014, the board was informed that the appellant would not attend the oral proceedings.

Oral proceedings were held on 18 September 2014 in the absence of the appellant.

IV. Claim 1 of the appellant's main (and sole) request reads as follows:

"*A high electron mobility transistor (HEMT) comprising:*
a semi-insulating silicon carbide substrate;
an aluminum nitride buffer layer (12) on said semi-insulating silicon carbide substrate;
an insulating gallium nitride layer (13) on said aluminum nitride buffer layer;
an active structure (14) of aluminum gallium nitride on said insulating gallium nitride layer; and

respective source, drain and gate contacts (20, 21, 22) to said aluminum gallium nitride active structure, characterized by a passivation layer (23) for enhancing the flow of electrons in said active structure, said passivation layer being selected from a group consisting of silicon dioxide or silicon nitride on said aluminum gallium nitride active structure, said passivation layer covering contact portions of the source, drain and gate contacts and possessing windows to permit electrical connections to said source, gate and drain contacts."

V. The appellant submitted in substance the following arguments:

Document D1 did not disclose a passivation layer as claimed. Document D3 generally related to field effect transistors that included a passivation layer. In particular, D3 disclosed a device having gate, drain, and source regions along with a passivation layer disposed over the gate, drain, and source regions. According to D3, the passivation layer functioned to prevent oxidation of various layers of the device in Figure 1. However, claim 1 recited a passivation layer for enhancing the flow of electrons in an active structure. D3 did not disclose that the passivation layer functioned to enhance the flow electrons. Instead, the passivation layer merely functioned to prevent oxidation. Moreover, the mere fact that the device of D3 included the passivation layer did not mean that the passivation layer enhanced the flow of electrons such that the feature of claim 1 noted above lacked inventiveness. As one skilled in the art would readily recognize, a passivation layer should include additional material features that enhanced electron flow. Thus, one skilled in the art would readily

appreciate that merely placing a passivation layer over a device would not enhance electron flow. Accordingly, claim 1 was patentable over the cited references.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments

Claim 1 as amended is based on claim 1 as originally filed and on the description as originally filed (cf page 7, first and third paragraphs).

Accordingly, the amendments comply with Article 123(2) EPC.

3. Novelty

A transistor according to the pre-characterising portion of claim 1 is known from document D1.

In particular, D1 discloses a Heterostructure Field Effect Transistor (HFET), which is a High Electron Mobility Transistor (HEMT), comprising:
a semi-insulating silicon carbide substrate (SiC);
an aluminum nitride buffer layer (AlN) on said semi-insulating silicon carbide substrate;
an insulating gallium nitride layer (i-GaN)) on said aluminum nitride buffer layer;
an active structure (AlGaN) of aluminum gallium nitride on said insulating gallium nitride layer; and

respective source, drain and gate contacts to said aluminum gallium nitride active structure (cf page 492, left-hand column, first paragraph and figure 1).

Not disclosed in document D1 are the features in the characterising portion of claim 1, that is:

a passivation layer for enhancing the flow of electrons in said active structure, said passivation layer being selected from a group consisting of silicon dioxide or silicon nitride on said aluminum gallium nitride active structure, said passivation layer covering contact portions of the source, drain and gate contacts and possessing windows to permit electrical connections to said source, gate and drain contacts.

Accordingly, the subject-matter of claim 1 is new over document D1 (Article 54(1) EPC 1973).

The subject-matter of claim 1 is also new over the remaining available prior art.

4. *Inventive step*

The passivation layer generally protects the device from the environment. The windows in the passivation layer permit making the necessary electrical connections to the source, gate and drain contacts. The effect of these distinguishing features thus is providing the essential protection of the device.

The objective problem to be solved relative to document D1, thus, may be formulated as protecting the device of D1.

The formulation of this problem does not require any inventive skills. It would be readily apparent to a person skilled in the art, working in the field of semiconductor devices, that the device of D1 needs protection.

Moreover, from document D3 it is known to form a passivation layer on a semiconductor device in order to protect the device and to avoid the introduction of impurities from the ambient into the device (cf column 1, lines 33 to 40). In particular, it is known from document D3 to provide a silicon nitride passivation layer on a GaAs FET, where the passivation layer is formed over the source, drain and gate contacts (cf column 3, line 20 to column 4, line 42; figure 1). The provision of openings to these contacts would be obvious to the skilled person in order to permit providing the necessary electrical connections to these contacts.

The appellant argued that document D3 did not disclose a passivation for enhancing the flow of electrons in an active structure of a transistor. In particular, the mere fact that the device of D3 included the passivation layer 6 did not mean that the passivation layer 6 enhanced the flow of electrons. As one skilled in the art would readily recognize, a passivation layer should include additional material features that enhance electron flow. Thus, one skilled in the art would readily appreciate that merely placing a passivation layer over a device would not enhance electron flow.

It is, however, noted that claim 1, and indeed the application as a whole, is silent about any such "*additional material features that enhance electron*

flow". Claimed and otherwise disclosed in the description is merely a passivation layer of either silicon dioxide or silicon nitride. According to the description, "*it appears that unterminated chemical bonds at the surface of a high-frequency device with a rectifying metal contact can create charge states that disrupt device operation by trapping a proportion of the electrons that would otherwise flow in the channel of a MESFET, or in the 2DEG of a HEMT. The passivation layer 23 of the present invention appears to minimize or eliminate this and similar problems*" (cf page 7, lines 7 to 13). There is no indication in the application that the passivation layer used would differ from a standard, per se well-known passivation layer of silicon dioxide or silicon nitride. Indeed, there is no disclosure whatsoever of which additional material features this layer should have and how these additional material features should be produced.

Accordingly, it is understood that the silicon nitride passivation layer of document D3, when provided over the device of D1 will have the same effect of enhancing the flow of electrons in the active structure.

Accordingly, the subject-matter of claim 1, having regard to the state of the art, is obvious to a person skilled in the art, Article 56 EPC 1973.

5. *Request for reimbursement of the appeal fee*

The appellant requested the reimbursement of the appeal fee by reason of a substantial procedural violation in the first instance proceedings (Rule 103(1)(a) EPC). The appellant argued that the examining division apparently did not examine the subject-matter of the dependent claims, and went straight to giving an

Article 56 refusal decision on the first auxiliary request without passing any comment on the dependent claims at all. This deprived the applicant of the opportunity to come to an allowable set of claims in front of the examining division.

There is, however, no requirement on the examining division to deal with dependent claims where the independent claim is found not be allowable. No procedural violation is, therefore, seen to have taken place.

For the above reasons, and as the appeal is also on substantive issues not deemed allowable, the appellant’s request for reimbursement of the appeal fee is refused (Rule 103(1)(a) EPC).

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated