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Datasheet for the decision of 4 March 2016

Case Number: T 2290/10 - 3.5.07

Application Number: 99915037.8

Publication Number: 0985214

IPC: G11C16/06

Language of the proceedings: EN

Title of invention:
Flash memory rewriting architecture having no external latch

Applicant:
Lexar Media, Inc.

Headword:
Flash memory/LEXAR MEDIA

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - (no) all requests

Decisions cited:

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Catchword:

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D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 2290/10 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 4 March 2016

Appellant: (Applicant)	Lexar Media, Inc. 47421 Bayside Parkway Fremont, CA 94538 (US)
Representative:	Beresford, Keith Denis Lewis Beresford Crump LLP 16 High Holborn London WC1V 6BX (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 16 July 2010 refusing European patent application No. 99915037.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Moufang
Members:	P. San-Bento Furtado
	R. de Man

Summary of Facts and Submissions

I. The appeal lies from the decision of the Examining Division to refuse European patent application No. 99915037.8, filed as international application PCT/US99/06572 and published as WO 99/49470, for lack of inventive step, Articles 52(1) and 56 EPC, of the subject-matter of all claims 1 to 5 of the then sole request over document D2 in combination with document D1:
D1: US 5 715 423 A, published on 3 February 1998;
D2: US 5 341 330 A, published on 23 August 1994.

II. In previous communications the Examining Division had also cited document D3:
D3: US 5 353 256 A, published on 4 October 1994.

III. In the notice of appeal, the appellant requested that the decision be set aside and that a patent be granted. In the statement of grounds of appeal, the appellant maintained the set of claims of the request considered in the contested decision.

IV. The appellant was invited to oral proceedings. In a subsequent communication, the Board expressed its preliminary opinion that the subject-matter of claim 1 did not involve an inventive step over the disclosure of document D2 in combination with the teaching of document D1. The same appeared to be the case when taking as a starting point either document D1 or the generic multiple flash memory array system as known at the date of priority of the application. The Board pointed at some possible issues for discussion at the oral proceedings with regard to the questions of lack of clarity and added subject-matter. The Board also reminded the appellant of the lack of unity objection

raised during the first instance proceedings and possible consequences with regard to admitting future requests.

V. By letter of reply dated 4 February 2016, the appellant submitted a replacement set of claims 1 to 5. With a further letter of 2 March 2016, the appellant submitted two further sets of claims as first and second auxiliary requests and amended description pages 1 to 13.

VI. Oral proceedings were held on 4 March 2016. At the end of the oral proceedings, the chairman pronounced the Board's decision.

VII. The final requests of the appellant were that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request filed with the letter of 4 February 2016 or, in the alternative, on the basis of the claims of one of the first and second auxiliary requests filed with the letter of 2 March 2016.

VIII. Claim 1 of the main request reads as follows:

"A flash memory system (200) comprising:

a plurality of flash arrays (205) each divided into a plurality of memory blocks for storing data;

a plurality of internal latches (210) coupled to each of the flash arrays (205) for temporarily holding data previously stored at a source address of a first flash array (205) of the plurality of flash arrays (205);

an internal controller (240) coupled to the first flash array (205) and the plurality of internal latches (210) coupled thereto and configured to transfer the data previously stored at the source address of the

first flash array (205) to the plurality of internal latches (210) and then to directly transfer the data previously stored at the source address of the first flash array (205) to a destination address in the first flash array (205); and

an external controller (135) coupled to the plurality of flash arrays (205) and configured to initially search within the first flash array (205) for a free memory block for use as the destination address, said external controller (135) being further configured to search for a free memory block in the remaining flash arrays (205) of the plurality of flash arrays (205) only in response to the external controller (135) not finding a free memory block in the first flash array (205); and

the external controller (135) also being configured to transfer the data previously stored at the source address of the first flash array (205) to an external buffer (141) and to write the data previously stored at the source address of the first flash array (205) from the external buffer to the free memory block in the one of the remaining flash arrays (205), when the external controller (135) finds a free memory block in one of the remaining flash arrays (205)."

IX. Claim 1 of the first auxiliary request differs from claim 1 of the main request in that the last part of the claim starting with "an external controller (135) coupled to the plurality of flash arrays (205)" has been replaced by the following text:

"an external controller (135) coupled to the plurality of flash arrays (205);
wherein

said external controller is configured to be responsive, upon receiving a write command,

to determine (730) whether or not all sectors within an addressed block of said first flash array are to be updated,

if all sectors within the addressed block are to be updated, to proceed (740) by writing new data to a new block; but

if not all sectors within the addressed block are to be updated to initially search within the first flash array (205) for a free memory block for use as the destination address, otherwise to search for a free memory block in the remaining flash arrays (205) of the plurality of flash arrays (205) only in response to the external controller (135) not finding a free memory block in the first flash array (205), and to transfer the data previously stored at the source address of the first flash array (205) to an external buffer (141) and to write the data previously stored at the source address of the first flash array (205) from the external buffer to the free memory block in the one of the remaining flash arrays (205), when the external controller (135) finds a free memory block in one of the remaining flash arrays (205)."

X. Claim 1 according to the second auxiliary request adds to the end of claim 1 of the first auxiliary request the following text:

"but

if said external controller (135) upon searching finds (790) no free memory block in any one of the remaining flash arrays (205), said external controller is to report (810) that no space is available."

XI. The appellant's arguments relevant to the decision are discussed in detail below.

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

2. *The invention*

2.1 The application is directed to "flash memory devices that do not utilize an external memory device to perform a rewrite operation within the flash memory device" for eliminating "the extra overhead of saving the data to be rewritten onto the external memory device" (page 1, lines 6 to 8 and page 4, lines 20 to 22 of the international publication).

2.2 As explained in the application, data stored in a flash memory cannot simply be changed as is done in rewrite or update operations in other conventional forms of memory. In order to change a programmed bit in a flash memory, the bit has to be erased and then reprogrammed. A flash memory is typically arranged in blocks, each block including a plurality of addressable sectors.

According to the application, in a conventional flash memory system, data in a memory block is changed by first reading out the data stored in that block (the source block) from the flash memory and storing it in an external buffer, then identifying a free block as destination block, copying the unchanged sectors to corresponding sectors of the destination block, and programming the changed data directly to the remaining sectors of the destination block (page 1).

In order to transfer unchanged data from the source block to the destination block, the data is first read

onto a flash data latch. A controller then sequentially reads the data from the latch, e.g. one byte at a time, and stores it onto an external memory or external buffer. Afterwards it sequentially reads the data, e.g. one byte at a time, from the external buffer, writes it back onto the flash data latch and from there to the destination block inside the flash array of the flash memory device. In conventional flash memory devices, the steps of sequentially shifting data between the flash data latch and the external buffer are time-consuming, degrading the performance of the device (page 1, line 24 to page 2, line 15).

2.3 In order to obviate that problem, in one embodiment the device of the invention uses a destination address latch and a source address latch, and a new "move" command, for writing unchanged data from a source block to a destination block without temporarily storing the data to be rewritten in an external memory. An internal buffer is used for the intermediate storage. The invention hence provides more efficient data rewrite operations by eliminating the need for sequentially shifting data to and from the external memory (page 8, line 6 to page 9, line 7, Figure 5).

2.4 A further embodiment relates to a flash memory system having several flash arrays. If there are no free blocks in the flash array of the source block during a rewrite operation, but a free block is found in another flash array which can be used as destination block, the data of the source block is stored temporarily in an external memory and then written to the destination block in the other flash array (page 9, line 24 to page 10, line 18, Figure 7).

2.5 The claims of the main request relate to a flash memory system and a method for transferring data from a first memory block to a second memory block, the flash memory system having a plurality of flash arrays. The same applies to the claims considered in the decision under appeal and by the Board in its preliminary opinion.

Claim 1 of each of the auxiliary requests is directed to a multiple flash memory array system configured for carrying out a rewrite operation by means of a write command for updating data. The additional features were taken from the embodiment of Figure 7 described on page 9, line 24 to page 10, line 18.

Main request

3. Inventive step

3.1 Document D2, considered as the closest prior art by the Examining Division, discloses a flash memory system for long-term storage of data (column 1, lines 10 to 15 and 32 to 49). As disclosed in column 2, lines 1 to 6, column 4, lines 28 to 53, and Figure 1, the flash memory system of D2 comprises a plurality of chips (11) for storing data, each chip including a number of blocks (B0, B1, ...).

The Examining Division considered each chip (11) of document D2, instead of the memory array (10), to correspond to a flash array as recited in the claim. The Board agrees with this mapping of features, which was not contested by the appellant. In the context of the present application, an array is a unit of memory with an internal command and control logic, the same applying to each of the chips of the memory system of document D2. In particular, document D2 mentions in

column 4, lines 51 to 53, that in one embodiment each chip has its own command and write state machines. The Board follows the Examining Division in considering that a command and write state machine of a memory chip of D2 constitutes an internal controller as recited in claim 1 of the main request.

3.2 Document D2 explains in column 2, lines 1 to 9, that a flash memory array is divided into smaller separately erasable blocks. When data in a sector is updated, the changed information is written to a new sector on an available block and the old sector is marked dirty.

In the multiple flash memory system of document D2, the number of dirty sectors in a block increases with time. Since dirty sectors cannot be used for storage, after some time a block with dirty sectors, i.e. a dirty block, has to be freed to provide space for new data. The dirty block is then erased and put back into use as a clean block of memory.

In order to erase a dirty block and release it to be used as a clean block of memory, first the still valid data in the dirty block to be erased is written to a new block, and then the dirty block is erased (column 2, lines 10 to 33; column 5, lines 37 to 51). The Board considers this transfer of data from the block to be erased to the new block to correspond to a data transfer according to the claim.

Document D2 does not explain whether the destination blocks to which the data is transferred prior to erasure are in the same chip or not. However, in the opinion of the Board, the skilled person would understand from the disclosure of document D2 that a

destination block may be either in the same chip or in another chip.

At the oral proceedings, the appellant argued that document D2 disclosed a different way of writing data to a block of the flash memory. The Board recognises that the approach for updating data in a block in the multi-flash memory of document D2 is distinct from that of the present application. Instead of copying to the destination block both the unchanged sectors of the original block and the updated sectors, the system of document D2 marks sectors with outdated data dirty and uses new sectors for the updated data. However, claim 1 of the main request only recites the steps needed to find a free memory block and transfer data to the new block and hence does not relate to data updating (see also point 2.5 above). Although the present application explains that a transfer of data between blocks is necessary when updating data, the claim does not specify any steps directly related to updating data and is therefore not restricted to transfer operations in the context of a rewrite operation. Since, furthermore, document D2 describes transfers of data between blocks, it is an adequate starting point for the assessment of inventive step of claim 1 of the main request.

3.3 During the erasure operation, which may take a long time, write operations to the blocks of a chip of the array in which the erasure is taking place are not allowed. The system of D2 solves this problem by writing the changed data to blocks on chips other than the chip containing the block being erased. This solution is also explained in the passage of column 7, lines 4 to 13, cited by the Examining Division and by the appellant, the first two sentences of which read "It is, however, possible to write changed data

originally stored on the chip containing the block being erased to blocks on other chips. The write state machine simply finds unused space on another chip in the array and writes to that space". Furthermore, the memory system of D2 includes a controller or read and write control circuit (14) associated with a command state machine and a write state machine coupled to the plurality of chips (see column 4, lines 33 to 51, Figure 1). The control circuit is also responsible for finding free space when transferring data of a block which will be erased (column 8, lines 10 to 13). Therefore, document D2 discloses the claimed feature "said external controller (135) being further configured to search for a free memory block in the remaining flash arrays (205) of the plurality of flash arrays (205)".

3.4 The following features therefore distinguish the claimed subject-matter from the flash memory system of document D2:

(a) a plurality of internal latches coupled to each of the flash arrays for temporarily holding the data to be transferred;

(b) the internal controller being configured to transfer the data stored in a source address of the first flash array to the plurality of internal latches and then to directly transfer the data to a destination address in the first flash array;

(c) the external controller being configured to initially search within the first flash array for a free memory block for use as the destination address and searching in the remaining flash arrays in response to not finding a free memory block in the first flash array.

Additionally, document D2 does not give details about the way data is transferred between different flash arrays. In particular, it does not disclose whether an external buffer is used as recited in the claim. However, that feature of the claimed system does not interact with features (a) to (c) above, and is not relevant to the improvement targeted by the invention with respect to transfers of data within an array. Furthermore, the claim does not specify what the external buffer is. In view of that, the external buffer constitutes a minor implementation option as found in conventional flash memory systems (see also point 2.2 above).

3.5 In the Board's view, features (a) to (c) solve the problem of improving the efficiency of data transfer operations in the multi-flash memory device of document D2.

3.6 Document D1 discloses a non-volatile flash memory system (column 1, lines 15 to 25) and deals with the problem of inefficient data transfer operations in those memories (column 1, lines 26 to 48).

In the grounds of appeal and at the oral proceedings, the appellant argued that the skilled person would not combine the teachings of D1 and D2 because the system of D1 performed write commands in a very different way, namely by transferring the data to another block. Document D2 disclosed a complete solution to the problem as a whole and did not give any motivation to deviate from its explicit teaching. The Board does not find this argument persuasive because claim 1 of the main request is not about updating data. The problem posed regards data transfers between blocks in a flash memory system, independently of the context in which

the transfer takes place (see also point 3.2 above). The same problem is addressed by document D1.

The Board is therefore of the opinion that the skilled person starting from the multiple flash memory array system of D2, and faced with the problem of speeding up data transfer operations, would take into account the teaching of document D1, which is directed to flash memory systems.

3.7 The solution suggested by document D1 consists of transferring the data directly within the memory chip, in particular by moving the data from the source block of memory to an internal page buffer and then to the destination block (abstract, column 4, line 59 to column 5, line 19). Document D1 therefore discloses features (a) and (b) used for the same purpose of speeding up data transfers within a flash memory.

In order to achieve that effect in the memory device of document D2 the skilled person would hence consider adopting the solution of document D1, i.e. adding an internal latch or buffer to each memory chip for directly transferring data from one source block to a destination block within the same chip.

Moreover, since transfers within a memory chip are faster using the idea of document D1, it would be obvious for the skilled person trying to integrate the solution of document D1 in the multiple flash memory array device of document D2 to configure the controller to search for a destination memory block in the same chip, i.e. in the same "array" in the terminology of the claim, before searching for a block in a different chip, as in feature (c).

3.8 In summary, the skilled person confronted with the problem of improving the efficiency of transfer operations in the multiple flash memory array system of document D2 would consider the teaching of document D1 and add features (a) and (b) of the flash memory of D1 to the memory system of document D2. Using its ordinary skills to integrate the solution of D1 in the multiple flash memory array system of D2, the skilled person would arrive at feature (c), obtaining a flash memory system as recited in claim 1.

3.9 The subject-matter of claim 1 of the main request therefore does not fulfil the requirements of Articles 52(1) and 56 EPC.

First auxiliary request

4. *Interpretation of claim 1*

4.1 The memory system of claim 1 of the first auxiliary request differs from that of the main request in that it is configured to perform a rewrite operation instead of solely transferring data (see also point 2.5 above).

The Board understands claim 1 of the first auxiliary request as reciting a multi-flash memory array system configured to process a write command to update data stored in an addressed memory block (the source block) essentially by

- first determining whether all sectors within the addressed block of the first flash array are to be updated and,
- if all sectors are to be updated, writing the new data to a new block,
  otherwise, the external controller searching for a free memory block to use as destination block

initially within the first flash array and, if none is free, in the remaining flash arrays,

- if the external controller finds a free memory block in one of the remaining flash arrays, transferring the data previously stored at the source address to the destination block through an external buffer.

4.2 Claim 1 of the first auxiliary request does not explain how data is rewritten to a block if not all sectors are to be updated and the external controller finds a free memory block in the first flash array, i.e. a destination block within the same memory array as the addressed block. In view of the description on page 10, lines 8 to 10, and Figure 7 (see feature 770), and page 8, line 30 to page 9, line 4, the Board understands that in that case the data is first transferred to the internal latches and then directly to the destination address as defined by the claim. The Board notes, however, that the claim does not establish the link between the write command and the data transfer within an array by the internal controller using internal latches.

5. Admission of the request

5.1 In its communication, the Board called the attention of the appellant to the fact that an objection regarding lack of unity had been raised during examination and that the history of the case might speak against admission by the Board of requests directed to the problem of updating data. Furthermore, the first auxiliary request was submitted late in the appeal proceedings, namely two days before the oral proceedings.

5.2 At the oral proceedings, the Board nevertheless decided to exercise its discretion under Article 13(1) RPBA in the appellant's favour and to admit the first auxiliary request. In its decision to admit the request, the Board took into account that it could treat the claims of the first auxiliary request without adjournment of the proceedings, and that the subject-matter of the first auxiliary request represented a further restriction of previously examined subject-matter. Furthermore, with the first auxiliary request the appellant addressed the deficiencies discussed by the Board in its communication, including preliminary objections raised for the first time with regard to clarity and added subject-matter.

6. *Inventive step*

6.1 Inasmuch as the memory system of document D2 performs rewrite operations in a completely different manner than that of claim 1 of the first auxiliary request, namely without transferring data of unchanged sectors of the original block to the destination block, it is not an adequate starting point for the assessment of inventive step of that claim.

In line with the explanation in its preliminary opinion, the Board finds the generic multiple flash memory array system, as known at the date of priority of the present application, to be an adequate starting point for assessing inventive step. That multiple flash memory array systems were known is confirmed by the disclosures of documents D2 and D3 (see document D3, abstract, Figure 2, column 3, lines 26 to 64).

Additionally, as pointed out at the oral proceedings, the application acknowledges that prior art. The

section dedicated to the background art on pages 1 to 3 describes a conventional flash memory device and its functionality (see also Figures 1 and 2). It explains how such a device updates data in a block by first reading the data in the source block to a buffer latch, programming those sectors that remain unchanged to a destination block and programming the changed data to other sectors of the destination block (page 1, lines 24 to 31). In the Board's view, the simple reference to "multiple flash memory array systems" on page 4, lines 26 to 27, without further explanation of the term, also means that the applicant considered such systems to be well known. The appellant did not contest that multiple flash memory array systems were acknowledged in the application and well known.

6.2 The multiple flash memory array system acknowledged in the application has to be understood as including a plurality of conventional arrays of the type depicted in Figure 1 (see also document D3, column 3, lines 54 to 56), and as being configured to update data in the conventional way explained under points 2.2 and 6.1 above, namely, by transferring unchanged sectors of the source block to a destination block and directly writing the data of changed sectors to the destination block (page 1, lines 24 to 31). It follows that if all the sectors are to be updated, the prior-art memory system proceeds to write the new data to a new block, as recited in the claim.

It is obvious that during updates in a multiple flash memory system, data may be transferred either within one array or between different arrays. In the latter case, an external controller is required to control operations of the whole device and in particular to transfer data between different arrays. Such an

external controller is coupled to the plurality of flash arrays and configured to transfer data from a source to a destination block. The Board further notes that, as pointed out by the Examining Division in its communication of 2 March 2010, an external controller is also present in the memory device of D3 (Figure 2, reference sign 332).

The typical flash memory array described in the present application on page 2, line 16 to page 3, line 2, and shown in Figure 1, also includes internal latches which, as explained in that passage of the description, are used for temporarily holding data when transferring data from one source address to a destination block, even if an external buffer is used for the transfer. Furthermore, in the Board's view an external buffer was standard in the well-known multiple flash memory arrays at the date of priority of the present application. The Board further notes that internal and external buffers are described with respect to the multiple memory array system of document D3 (see column 3, lines 41 to 64, column 6, lines 18 to 23, Figures 2 and 3, reference signs 70 and 330).

From the above it follows that, at the priority date of the present application, multiple flash memory arrays were known which included a plurality of internal latches for temporarily holding data when transferring data from one source address to a destination block, an external buffer, and an external controller.

6.3 Claim 1 of the first auxiliary request further specifies that

(i) the claimed memory system includes an internal controller coupled to the first flash array and to the plurality of internal latches, the

internal controller being configured to transfer the data previously stored at the source address of the first flash array to the plurality of internal latches, and then to directly transfer the data previously stored at the source address of the first flash array to a destination address in the first flash array; and

(ii) the external controller is further configured to be responsive, upon receiving a write command, to determine whether all sectors within the addressed block are to be updated and, if not all sectors are to be updated, to initially search within the first flash array for a free memory block for use as the destination address, and otherwise to search for a free memory block in the remaining flash arrays of the plurality of flash arrays.

These distinguishing features solve the technical problem of efficiently updating data in a multiple flash memory array system.

6.4 Document D1 discloses a non-volatile flash memory system for efficient transfer of data between blocks (see also points 3.6 and 3.7 above). In the opinion of the Board, the skilled person would hence take the teaching of document D1 into account in order to solve the problem mentioned above.

At the oral proceedings, the appellant argued that document D1 did not point to multiple flash memory arrays and that there was no reference to the problem of running out of storage space in an array. These arguments are not relevant to the present reasoning, which does not take the single array of document D1 as closest prior art, but a well-known multiple flash

memory array system, which includes an external buffer. The fact that the device of document D1 does not use an external buffer for data transfers in a memory device consisting of a single array does not mean that it teaches away from using external buffers for transfers between different arrays in a multiple flash memory array device.

The appellant also submitted that the usual thing to do in a multiple array system was to distribute data so that an array did not become full. The Board, on the contrary, considers that the skilled person would recognise the advantages of storing related data in the same array, especially in the light of the teaching of document D1.

As explained under point 3.7 above, document D1 discloses features (i) as a solution to the problem of efficiently transferring data in a flash memory array. The skilled person would therefore, without exercise of inventive skills, consider employing the technique of document D1 to implement efficient data updates in the known multiple flash memory system.

It would be obvious for the skilled person that in order to take advantage of the benefit brought about by the technique of document D1 in the context of a multiple flash memory, it would be preferable to transfer data within an array instead of between arrays (see also point 3.7 above). The skilled person would also immediately recognise that the update algorithm could be implemented within the external controller, for example as a write command. The skilled person would therefore, in the process of integrating those advantageous features in the known multiple flash memory array system, as a matter of routine, consider

adapting the external controller in the way recited in the claim according to features (ii).

6.5 From the above reasoning it follows that the subject-matter of claim 1 of the first auxiliary request does not involve an inventive step (Articles 52(1) and 56 EPC).

Second auxiliary request

7. Claim 1 of the second auxiliary request further recites that when the external controller finds no free memory block in any one of the remaining flash arrays, it reports that no space is available.

8. The Board decided to admit the second auxiliary request into the appeal proceedings for the same reasons as given for the first auxiliary request under point 5 above, and because the additional feature corresponds to a minor modification of the subject-matter of claim 1 of the first auxiliary request.

9. *Inventive step*

9.1 If the external controller cannot find a free memory block in any of the remaining flash arrays, after it could not find one in the first flash array, then the write command cannot be carried out. The function of the additional feature is to report a failure to perform the required operation. Such error indications are common practice in electronic devices and are required for error handling. Since, furthermore, no synergistic effect results from the combination of the error reporting feature with the remaining features of the claimed flash memory system, the feature constitutes an obvious minor implementation detail.

9.2 The Board therefore finds that the second auxiliary request does not comply with Articles 52(1) and 56 EPC for lack of inventive step of the subject-matter of claim 1.

Concluding remarks

10. It is clear from the reasoning with respect to the auxiliary requests that the Board would, as mentioned in the oral proceedings, have arrived at the same conclusion with respect to inventive step of the main request, had it taken the well-known multiple flash memory array system as starting point for assessing inventive step of claim 1 of the main request.

11. As none of the appellant's requests is allowable, the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

I. Aperribay R. Moufang

Decision electronically authenticated