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Datasheet for the decision of 14 January 2016

Case Number: T 0104/11 - 3.5.07

Application Number: 99118540.6

Publication Number: 1033721

IPC: G11C7/22, G11C7/00, G11C16/32, G11C16/26, H03K5/13

Language of the proceedings: EN

Title of invention:
Programmable delay control in a memory

Applicant:
Freescale Semiconductor, Inc.

Headword:
Programmable delay/FREESCALE SEMICONDUCTOR

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
Claims - clarity - main request (no)
Inventive step - auxiliary request I (yes)

Decisions cited:

Catchword:

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Case Number: T 0104/11 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 14 January 2016

Appellant: (Applicant)	Freescale Semiconductor, Inc. 6501 William Cannon Drive West Austin, TX 78735 (US)
Representative:	Wray, Antony John Optimus Patents Limited Grove House Lutyens Close Chineham Court Basingstoke Hampshire RG24 8AG (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 3 September 2010 refusing European patent application No. 99118540.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Moufang
Members:	R. de Man
	M. Rognoni

Summary of Facts and Submissions

I. The applicant (appellant) appealed against the decision of the Examining Division refusing European patent application No. 99118540.6.

II. The decision cited the following documents:

D1: EP-A-0 668 591, 23 August 1995;
D2: GB-A-2 316 208, 18 February 1998;
D3: JP-A-10 112182, 28 April 1998;
D4: EP-A-0 884 732, 16 December 1998;
D5: JP-A-10 334665, 18 December 1998; and
D6: US 5970014, 19 October 1999.

Document D6 was cited as a family member of document D5 in the English language.

The Examining Division decided on a main request, an unamended auxiliary request 1, an amended auxiliary request 1, an auxiliary request 2, an auxiliary request 3, and an unamended auxiliary request 4.

III. With the statement of grounds of appeal, the appellant submitted a main request and first to third auxiliary requests.

IV. In a communication accompanying a summons to oral proceedings, the Board noted that various procedural irregularities had occurred during the first-instance proceedings, but that there appeared to be no reason for a remittal of the case without substantive examination. With respect to the main request, it expressed the preliminary opinion that the subject-matter of claim 1 of the main request lacked inventive step *inter alia* in view of the common general knowledge of the skilled

person and raised the question whether claim 1 was clear.

V. With a letter dated 9 December 2015, the appellant commented on the Board's communication.

VI. In the course of oral proceedings held on 14 January 2016, the appellant submitted a new auxiliary request I comprising claims 1 to 4 and maintained the first to third auxiliary requests as auxiliary requests II to IV. At the end of the oral proceedings, the chairman pronounced the Board's decision.

VII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or, in the alternative, on the basis of one of auxiliary requests I to IV.

VIII. Claim 1 of the main request reads as follows:

"A memory comprising:
a plurality of memory blocks (17, 18);
a first selection circuit (24) that has an output which provides a first selection signal (62) that indicates a first delay; and
a first plurality of programmable delay circuits (40), each programmable delay circuit (40) being coupled to the output of the first selection circuit (24) for receiving the first selection signal (62), each programmable delay circuit (40) having an output, each output being associated with a memory block of the plurality of memory blocks (17, 18)."

IX. Claim 1 of auxiliary request I reads as follows:

"A memory comprising:

a plurality of memory blocks (17, 18, 70), each of which has a block control circuitry (21, 22, 72) with a sense amplifier (46) being a dynamic amplifier;

a first selection circuit (24) that has an output which provides a first selection signal (62) that indicates a first delay; and

a first plurality of programmable delay circuits (40),

each programmable delay circuit (40) being arranged in or in close proximity to a respective one of the plurality of memory blocks (17, 18, 70),

each programmable delay circuit (40) being coupled to the output of the first selection circuit (24) for receiving the first selection signal (62), and

each programmable delay circuit (40) having an output to enable the sense amplifier (46) of the block control circuitry (21, 22, 72) of the respective one of the plurality of memory blocks (17, 18, 70)."

Claims 2 to 4 are dependent on claim 1.

X. The text of auxiliary requests II to IV is not relevant to this decision.

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

2. *Procedural issues*

As discussed in detail in the Board's communication, during the first-instance proceedings leading up to the contested decision a number of procedural irregularities occurred. Since the appellant did not contest the Board's preliminary opinion that its interests had not been harmed by how the Examining Division had proceeded, there is no need to examine these points further in the present decision.

3. *The application*

The background section of the description explains that one of the difficulties in designing a memory circuit is optimising the timing of the clock signals that enable various functions in the memory circuit. One known approach is to provide programmable delay elements which may be programmed by means of fuses.

More specifically, timing considerations play a role in the use of dynamic sense amplifiers for reading data from memory cells. A dynamic sense amplifier consumes less power than a static sense amplifier, but whereas the latter amplifies any given signal at any given time, the former must be enabled exactly at the right time for optimal functioning. If a dynamic sense amplifier is enabled too late, there is a speed penalty; if too soon, reliability becomes an issue.

The application proposes a particular arrangement of programmable delay circuits for optimising the use of dynamic sense amplifiers.

4. *Main request - clarity*

4.1 Claim 1 of the main request relates to a memory comprising a "selection circuit" that has an output connected to a plurality of "programmable delay circuits". The selection signal output by the selection circuit indicates the delay with which the delay circuits are programmed.

The claim further specifies that the memory comprises a plurality of memory blocks and that each programmable delay circuit has an output that is "associated with a memory block of the plurality of memory blocks".

4.2 In its novelty analysis of claim 1 of the then main request (which is identical to claim 1 of the present main request), the Examining Division considered that document D1 disclosed a plurality of programmable delay circuits, each having outputs that indirectly controlled the timing of a number of sense amplifiers. These sense amplifiers were coupled to a memory cell array which could be seen as comprising a plurality of memory blocks. Each programmable delay circuit output was therefore "associated with a memory block of the plurality of memory blocks".

4.3 Relying on Figures 1 and 2 of the application, the appellant explained that according to the invention each programmable delay circuit of the plurality of programmable delay circuits corresponded to a respective memory block of the plurality of memory blocks and that the output of each programmable delay circuit fed certain circuit elements in block control circuitry of its respective memory block. In document D1, each programmable delay circuit output instead supplied *all* the "memory blocks" of the memory cell array.

4.4 The Board agrees with the appellant that document D1 does not disclose the specific arrangement of programmable delay circuits and memory blocks shown in Figures 1 and 2, which provide the only support for claim 1. But the claim wording "each output being associated with a memory block of the plurality of memory blocks", taken on its own, is sufficiently broad to encompass the arrangement shown in document D1. In the Board's view, the skilled person reading claim 1 in the light of the application as a whole may well reject that broad reading of the feature and would, in any event, have doubts about the precise technical limitation implied by it. This means that claim 1 is not clear within the meaning of Article 84 EPC.

5. *Auxiliary request I - admission*

Auxiliary request I was filed at the oral proceedings as a result of a discussion of Figures 1 and 2 of the application. Although the request represented a considerable amendment of the appellant's case, it overcame the Board's objections and raised no issues that the Board could not deal with without adjournment of the oral proceedings. The Board therefore decided to exercise its discretion under Article 13(1) RPBA and to admit the request into the proceedings.

6. *Auxiliary request I - clarity*

Claim 1 of auxiliary request I clarifies how programmable delay circuits are "associated with" memory blocks. Thus this request overcomes the lack of clarity of claim 1 of the main request.

7. *Auxiliary request I - added subject-matter*

7.1 The application as filed discloses, with reference to Figure 1, a memory comprising a plurality of memory blocks 17 and 18, each memory block including block control circuitry 21 and 22 (page 5, lines 4 to 9). The memory further comprises fuse circuitry 24, which has an output providing a signal 62, optionally comprising four binary data bits, to block control circuitry 21 and 22 (page 5, lines 16 to 18).

As explained on page 7, lines 1 to 17, with reference to Figure 2, block control circuitry 21 includes delay adjust circuitry 40, which receives signals 47 from fuse circuitry 24. It is evident that signals 47 correspond to (the data bits of) signal 62. The description on page 12, line 23, to page 13, line 18, and on page 15, lines 1 to 13, clarifies that the bits of signal 62 / signals 47 program the delay adjust circuitry of each block control circuitry with the same delay.

Each block control circuitry 21 further includes a sense amplifier 46, which is enabled by an output of the programmable delay circuit (Figure 2 and page 14, lines 15 to 23). The sense amplifiers 46 are dynamic amplifiers (page 20, lines 3 and 4).

7.2 Original claim 1 ("a selection circuit that has an output which provides a selection signal that indicates a delay") provides, in combination with original dependent claim 2 ("wherein the selection circuit comprises a plurality of fuses coupled together to provide the selection signal to indicate the delay"), a basis for the generalisation of fuse circuitry 24 to the "first selection circuit" of claim 1.

7.3 The description on page 17, lines 3 to 24, explains that other arrangements of the delay adjust circuitry relative to the memory block are possible, but that it is important to have a delay adjust circuitry in close proximity to each block. This provides a basis for the feature "each programmable delay circuit being arranged in or in close proximity to a respective one of the plurality of memory blocks".

7.4 The Board is therefore satisfied that the subject-matter of claim 1 is directly and unambiguously derivable from the application as filed.

7.5 Dependent claim 2 is based on page 6, lines 16 to 18, together with page 8, lines 17 to 21, of the original description.

7.6 Dependent claims 3 and 4 are based on original dependent claims 2 and 3, respectively.

7.7 Auxiliary request I hence complies with Article 123(2) EPC.

8. *Auxiliary request I - inventive step*

8.1 The subject-matter of claim 1 relates to a memory comprising a plurality of memory blocks, each block having block control circuitry including a dynamic sense amplifier. Each sense amplifier is enabled by a programmable delay circuit located in or close to the corresponding memory block. All programmable delay circuits are programmed with the same delay by means of a selection circuit.

8.2 In its decision, the Examining Division used both document D1 and document D5 as starting point for its

analysis of novelty and inventive step of the various requests on which it decided.

8.3 Document D1 discloses a timing circuit 1 forming part of a non-volatile memory 100 (column 1, lines 49 to 58, and Figure 1). The memory comprises *inter alia* a memory cell array 104 and an amplifying unit 105. The amplifying unit is formed by a number of sense amplifiers (column 2, lines 20 and 21).

Circuit 1 comprises a section 4, which comprises memory elements 20, 21 and 22 connected to adjustable asymmetrical delay units 23 and 24 (see column 3, lines 1 to 11 and 27 to 44). The delay units control timing aspects of the memory. Figure 1 shows that memory elements 20, 21 and 22 are fuses.

Adjustable asymmetrical delay unit 23 outputs a signal which is delayed with respect to an input signal, the delay depending on the content of memory elements 20 and 22 (column 3, lines 45 to 55). Similarly, the delay introduced by asymmetrical delay unit 24 depends on the content of memory elements 20 and 21 (column 4, lines 3 to 10).

8.4 Document D1 hence discloses the general idea of controlling timing aspects of a memory by means of adjustable delay units programmed by a set of fuses. But it does not disclose a plurality of memory blocks, each block having block control circuitry, and the delay units do not enable the sense amplifiers. Extensive modifications to the design of memory 100 would be necessary in order to arrive at a memory falling within the terms of claim 1, in particular if the delay units of document D1 are to have the role of the programmable delay units of claim 1.

8.5 Document D6 is a family member of document D5 in the English language. In view of the outcome of this decision, without further investigation it may be assumed that the content of document D6 corresponds to that of document D5, i.e. that it forms part of the prior art.

Document D6 discloses a semiconductor memory device comprising first and second memory blocks 10UB and 10DB comprising block control circuitry 40U and 40D and delay circuits 51 (column 4, lines 41 to 60; column 5, lines 11 to 20; Figure 3).

Since the delay circuits of the memory of document D6 are not programmable and do not enable sense amplifiers, this document likewise is not a good starting point.

8.6 Also documents D2, D3 and D4 are not particularly relevant to the invention as presently claimed. In the Board's view, a better starting point for the assessment of inventive step of the subject-matter of claim 1 than the cited prior art is the well-known general concept of a memory circuit comprising a plurality of memory blocks, each memory block having block control circuitry including a sense amplifier.

8.7 The subject-matter of claim 1 differs from this closest prior art in that

- the sense amplifiers are dynamic sense amplifiers;
- each sense amplifier is enabled by a programmable delay circuit located in or close to the corresponding memory block; and
- all programmable delay circuits are programmed with the same delay by means of a selection circuit.

8.8 As explained in the description of the application on page 17, lines 11 to 24, providing a separate programmable delay circuit in or close to each memory block reduces the inconsistency of delays compared to what could be achieved with one delay circuit in a single location on the chip, as that location would not be at the same distance to each memory block. And by locating the delay circuits close to the memory blocks, the effects of power supply voltage variations are reduced (page 17, line 24, to page 18, line 10).

In addition, by means of the selection circuit the delay may, after testing of the memory circuit, be optimised to a value that is long enough for all memory blocks to function reliably, but not longer than necessary (page 18, line 27, to page 19, line 13).

The objective technical problem solved by the distinguishing features may therefore be regarded as that of modifying the closest prior art to make efficient use of dynamic sense amplifiers.

8.9 The available prior art discloses various uses of programmable delay circuits in memory circuits, but it does not disclose a single selection circuit for programming the delay of a plurality of programmable delay circuits arranged to enable dynamic sense amplifiers.

The skilled person might under certain circumstances consider programming a plurality of programmable delay circuits by means of a single selection circuit providing a common delay, but the Board considers that neither the cited prior art, nor the common general knowledge, suggests using such an arrangement for

controlling the timing of dynamic sense amplifiers in order to achieve the above-mentioned advantages of the memory presently claimed.

It follows that the subject-matter of claim 1 involves an inventive step (Articles 52(1) and 56 EPC).

8.10 Since claims 2 to 4 are dependent on claim 1, their subject-matter is likewise inventive.

9. *Auxiliary request I - double patenting*

The Board is aware that claim 1 of auxiliary request I is similar in scope to claim 1 of granted patent EP 1 770 708 B1, which originated as a divisional application of the present application. Since the two claims are only similar - and not identical - in scope, the prohibition of double patenting does not apply.

10. *Conclusion*

In view of the above, the Board comes to the conclusion that the claims of auxiliary request I satisfy the requirements of the EPC. However, the description and drawings may still require adaptation.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent on the basis of claims 1 to 4 according to auxiliary request I, filed in the oral proceedings, and of drawings and a description yet to be adapted.

The Registrar: The Chairman:

I. Aperribay R. Moufang

Decision electronically authenticated