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# Datasheet for the decision of 5 September 2017

**Case Number:** T 0103/12 - 3.4.03

**Application Number:** 03024395.0

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**IPC:** H01L29/739, H01L29/745, H01L29/749, H01L29/10, H01L29/08

**Language of the proceedings:** EN

**Title of invention:**
Field effect type semiconductor device

**Applicant:**
TOYOTA JIDOSHA KABUSHIKI KAISHA

**Headword:**

**Relevant legal provisions:**
EPC 1973 Art. 56
EPC Art. 123(2)

**Keyword:**
Amendments - extension beyond the content of the application as filed (yes)
Inventive step - auxiliary request (yes)

**Decisions cited:**

**Catchword:**

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**Beschwerdekammern**
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**Case Number: T 0103/12 - 3.4.03**

# D E C I S I O N
## of Technical Board of Appeal 3.4.03
## of 5 September 2017

| | |
|---|---|
| **Appellant:** (Applicant) | TOYOTA JIDOSHA KABUSHIKI KAISHA<br>1, Toyota-cho,<br>Toyota-shi, Aichi-ken, 471-8571 (JP) |
| **Representative:** | Kuhnen & Wacker<br>Patent- und Rechtsanwaltsbüro<br>Prinz-Ludwig-Straße 40A<br>85354 Freising (DE) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 6 July 2011 refusing European patent application No. 03024395.0 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chairman** | G. Eliasson |
| **Members:** | S. Ward |
| | C. Heath |

## Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 03 024 395 on the grounds that it failed to meet the requirements of the EPC for the reasons given in the communications dated 9 April 2009, 19 January 2011 and 13 May 2011. In all three communications the claimed subject-matter was said not to involve an inventive step within the meaning of Articles 52(1) and 56 EPC.

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted based on the main request, or one of auxiliary requests 1–3, all filed with letter dated 28 July 2017, or according to auxiliary request 7 (one claim only) as filed at 15.50 during oral proceedings, a description filed during oral proceedings and figures 1–31 as originally filed.

III. The following documents cited by the Examining Division are referred to in this decision:

D1: EP 1 032 047 A2
D4: EP 1 065 710 A2
D6: EP 1 120 834 A2

IV. Claim 1 of the main request reads as follows:

*"A field-effect-type semiconductor device comprising: a channel region (103; 403) of a first-conductivity-type semiconductor (P) having a width d in a horizontal direction;*

*a first-conductivity-type emitter region (100; 400) being in contact with the channel region, and being a first-conductivity-type semiconductor ($P^+$) with higher concentration than that of the channel region;*
*a gate electrode (106; 406) penetrating the channel region, and insulated from the channel region and the first-conductivity-type emitter region;*
*an emitter electrode (109; 409) being in contact with the channel region and with the first-conductivity-type emitter region;*
*a second-conductivity-type emitter region (104; 404) being insulated from the gate electrode, the second-conductivity-type emitter region being a second-conductivity-type semiconductor ($N^+$),*
*wherein the second-conductivity-type emitter region is in contact with the channel region and the emitter electrode, and*
*the gate electrode, with a facing surface thereof, faces in the horizontal direction the second-conductivity-type emitter region, the channel region and a contact portion of those regions;*
*characterised in that*
*a ratio X/W is between 1/10 and 1/2,*
*wherein X denotes a vertical direction width of the second-conductivity-type emitter (104; 404) in a direction parallel to said facing surface, and*
*W is wider than the width X and denotes a vertical direction width of the channel region of the first conductivity-type semiconductor (103; 403;) in a direction parallel to said facing surface;*
*that said width X is 20 µm or less; and that*
*a width, in the horizontal direction perpendicular to said facing surface, of the first-conductivity-type emitter region (100; 400) is narrower than a width (108), in the horizontal direction perpendicular to said facing surface, where the emitter electrode (109;*

*409) is in contact with the channel region (103; 403) and with the first-conductivity-type emitter region (100; 400)."*

In auxiliary requests 1-3, claim 1 is similarly directed to a "field-effect-type semiconductor device" having essentially the features of claim 1 of the main request plus additional features.

Claim 1 of auxiliary request 7 reads as follows:

*"An insulated gate bipolar transistor (IGBT) with a trench-type gate structure comprising:*
*a channel region (103) of a first-conductivity-type semiconductor (P);*
*a first-conductivity-type emitter region (100) arranged on a surface side of a semiconductor substrate and being in contact with the channel region, and being a first-conductivity-type semiconductor ($P^+$) with higher concentration than that of the channel region;*
*the channel region (103) and the first-conductivity-type emitter region (100) constitute a first-conductivity-type region;*
*two gate electrodes (106) arranged linearly in a vertically striped pattern on the surface side of the semiconductor substrate and penetrating the channel region, and insulated from the channel region and the first-conductivity-type emitter region;*
*an emitter electrode (109) being in contact with the channel region and with the first-conductivity-type emitter region;*
*a second-conductivity-type emitter region (104) disposed on the surface side of the semiconductor substrate discretely between adjoining gate electrodes (106) and being insulated from the gate electrodes*

*(106), the second-conductivity-type emitter region being a second-conductivity-type semiconductor ($N^+$), the first-conductivity-type region and the second-conductivity-type emitter region (104) form a unit which is repeated in the vertical direction on the surface side of the semiconductor substrate; and*
*wherein the second-conductivity-type emitter regions are in contact with the channel region (103) and the emitter electrode (109), and*
*the gate electrodes, with a facing surface thereof, face in the horizontal direction the second-conductivity-type emitter regions, the channel region and a contact portion of those regions;*
*a ratio X/W is between 1/10 and 1/2,*
*wherein X denotes a vertical direction width of the second-conductivity-type emitter (104) in a direction parallel to said facing surface and parallel to the surface side of the semiconductor substrate, and*
*W denotes a vertical direction width of the first-conductivity-type region in a direction parallel to said facing surface and parallel to the surface side of the semiconductor substrate; and*
*said width X is 20 µm or less; and*
*a width, in the horizontal direction perpendicular to said facing surface, of the first-conductivity-type emitter region (100) is narrower than a width, in the horizontal direction perpendicular to said facing surface, where the emitter electrode (109) is in contact with the channel region (103) and with the first-conductivity-type emitter region (100)."*

V. The Board sent a communication under Article 15(1) RPBA with the summons to oral proceedings, and a further communication dated 30 August 2017. Objections under Article 123(2) EPC were raised, and the question of inventive step was discussed.

VI. The appellant's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

The amendments to claim 1 of the main request satisfied the requirements of Article 123(2) EPC. In particular, while claim 1 had been amended by including features taken from specific embodiments of the description, for example the ratio X/W being between 1/10 and 1/2, and the width X being 20 µm or less, the skilled person would appreciate that these features were not inextricably linked, structurally or functionally, with other features of the respective embodiments which had not been imported into claim 1, and so no intermediate generalisation arose.

Starting from the device of Fig. 16 of document D1, which was the closest prior art, there was nothing in the cited prior art which would lead the skilled person to the claimed invention.

## Reasons for the Decision

1. The appeal is admissible.

2. *Article 123(2) EPC*

2.1 Several features of claim 1 of the main request are not defined in any of the claims as originally filed, but are only disclosed in the description and drawings in relation to specific embodiments.

2.2 For example, according to claim 1, the "width X is 20 µm or less", a feature which was originally disclosed only in the passages on page 15, lines 13-16 and page 32, lines 4-7 in relation to the devices of Figs. 1-10 and Figs. 19-22 (referred to in the original description as the "first embodiment" and the "fourth embodiment", respectively).

These embodiments (in fact, all disclosed embodiments) are insulated gate bipolar transistors (IGBTs) with trench-type gate structures, whereas claim 1 of the main request is directed to a more general "field-effect-type semiconductor device". The question therefore arises whether the claimed combination of features represents a level of generalisation not originally disclosed - even implicitly - to the skilled reader.

2.3 The Board recognises that there is a very general statement in the original application that "the present invention is applicable to not only an IGBT but also other types of field-effect-type semiconductor devices..." (page 39, lines 20-23).

In a patent application in which the claims are directed to a general "field-effect-type semiconductor device", but in which the only described embodiments are IGBTs, the inclusion of such a statement is presumably intended to provide support in the description within the meaning of Article 84 EPC for the original claims.

In the opinion of the Board, however, this statement does not have any bearing on the question whether a feature which was not originally claimed, and which is disclosed only in the context of specific embodiments,

may subsequently be claimed in a more general context without violating the requirements of Article 123(2) EPC.

2.4 The feature that the width X is 20 µm or less is disclosed only in the two passages mentioned above, as follows:

> *"Furthermore, it is preferable that the width X of the $N^+$ emitter region ... is 20 µm or narrower. That is, in case it is too wide, latch-up phenomenon is likely to occur."*

The "latch-up phenomenon" referred to is that disclosed *inter alia* in the passage from page 4, line 15 to page 5, line 5, in terms of the device shown in Figs. 30 and 31, a device which the skilled person would immediately recognise as an IGBT. According to the description, this latch-up phenomenon is caused by the switching on of a parasitic NPNP thyristor comprising regions 904, 903, 902, and 901, (collector region 901 is wrongly referred to as "$N^+$" on page 5, line 2; clearly this should read "$P^+$", as on page 2, lines 14-17 and in Fig. 31).

This type of latch up is a well-known problem in IGBTs, but does not occur in other field-effect-type semiconductor devices which would nevertheless fall within the ambit of claim 1 of the main request. For example, power MOSFETs do not suffer from the particular type of latch up disclosed in the application since, in a power MOSFET, the region corresponding to the $P^+$ collector region 901 in Fig. 31 would be replaced by an $N^+$ drain region, and so no parasitic NPNP thyristor would be formed.

2.5 Hence, the original application discloses, in the first and fourth embodiments only, a first feature that the width X is 20 µm or less, in combination with a second feature that the device is an IGBT. Claim 1 of the main request incorporates the first feature but not the second.

The first feature is disclosed, however, as overcoming a problem of IGBTs, and hence a clear technical relationship is disclosed in the application as filed between the first and second features, and there is no disclosure of the first feature in any other context. The Board therefore takes the view that importing the second feature into claim 1 of the main request, while omitting the first, results in the skilled person being confronted with technical information not unambiguously disclosed in the application as originally filed. As a result, claim 1 of the main request fails to meet the requirements of Article 123(2) EPC.

2.6 In auxiliary requests 1-3, claim 1 is similarly directed to a "field-effect-type semiconductor device" having the feature that the width X is 20 µm or less. This subject-matter fails to meet the requirements of Article 123(2) EPC for the reasons mentioned above, *mutatis mutandis*.

2.7 Claim 1 of auxiliary request 7 is directed to an insulated gate bipolar transistor (IGBT) with a trench-type gate structure, and hence the above objection has been overcome. The other objections raised in the Board's communications are also considered to have been overcome.

In particular, claim 1 (which is now directed at the first embodiment only, as is reflected in the amended

description adapted to auxiliary request 7) now includes a definition of the direction of W and X which is consistent with that disclosed in the description and drawings, and it is explicitly stated that the device is based on repeating units, the unit being satisfactorily defined.

2.8 In view of these amendments, and the other explicit amendments to claim 1, as well as those features which a skilled person would understand to be implicit in the term "insulated gate bipolar transistor (IGBT) with a trench-type gate structure", as now defined in the claim, the Board is satisfied that claim 1 of auxiliary request 7 meets the requirements of Article 123(2) EPC.

3. *Inventive step: auxiliary request* 7

3.1 In the light of point 3.2 of the communication of 13 May 2011, which refers to point 4.1 of the communication of 19 January 2011, which in turn refers to point 4 of the communication of 9 April 2009, the application was apparently refused for lack of inventive step on the basis of a combination of documents D1 and D4 or a combination of documents D1 and D6.

3.2 Both the appellant and the Examining Division saw the "trench insulating gate type IGBT" of Fig. 16 (and paragraphs [0057] and [0058]) of document D1 as the closest prior art, and the Board sees no reason to differ.

3.3 The following features defined in claim 1 are identified with features disclosed in D1 as follows:

| **Claim 1** | **Fig. 16 of Document D1** |
|---|---|
| channel region (103) of a first-conductivity-type semiconductor | p-type base layer (4) |
| first-conductivity-type emitter region (100) | p+ layer (6) |
| first-conductivity-type region (constituted by channel region and first-conductivity-type emitter region) | not explicitly defined |
| gate electrodes (106) | gate (7) |
| emitter electrode (109) | source electrode (10) |
| second-conductivity-type emitter region (104) | n-type source layer (5) |

According to paragraph [0057] of document D1, the n-type source layer 5 is divided longitudinally into a plurality of areas (only two are shown in Fig. 16), and a part of the p-type base layer 4 is positioned between neighboring areas of the n-type source layer 5 (see Fig. 16). Thus the n-type source layer 5 and an adjacent part of the p-type base layer 4 appear to represent a unit which is repeated.

Hence, comparing claim 1 with Fig. 16 of document D1, the claimed width X may be identified with the longitudinal (into the page) width of the n-type source layer 5, and the claimed width W may be identified with the longitudinal width of the intervening portion of the p-type base layer 4. Regarding the dimensions of these widths, or their ratio, document D1 is silent.

In Fig. 16 of D1 there is also a "groove which is a contact hole 201" so that the "area La is divided into two areas by this groove" (paragraph [0057]). Although not shown in Fig. 16 (which represents a cut-away view), it is stated in paragraph [0057] that:

> *"even in the contact hole 201, the main electrode 10 (source electrode) is electrically connected to the n-type source layer 5 and the p-type base layer 4. At the bottom of the contact hole 201, the p+ layer 6 whose impurity density is higher than that of the p-type base layer 4 is formed and the p-type base layer 4 is electrically connected to the main electrode via the p+ layer 6."*

The electrode 10 therefore extends to the bottom of the groove or contact hole 210, where it is in electrical connection with the p+ layer 6, which runs along the bottom of the groove.

3.4 Claim 1 differs from the closest prior art at least in the following features (emphasis by the Board):

(a) a first-conductivity-type emitter region (100) arranged **on a surface side of a semiconductor substrate**;

(b) the first-conductivity-type region and the second-conductivity-type emitter region (104) form a unit which is repeated in the vertical direction **on the surface side of the semiconductor substrate**;

(c) a ratio X/W is between 1/10 and 1/2;

(d) said width X is 20 µm or less.

A further difference may be derived from the features:

(e) **a second-conductivity-type emitter region** (104) disposed **on the surface side** of the semiconductor

substrate discretely **between adjoining gate electrodes** (106) and being **insulated from the gate electrodes** (106) ...

Thus, for each repeat unit, the region 104 on the surface side of the semiconductor substrate is "a" (singular) second-conductivity-type [$N^+$] emitter region, which is disposed between, and adjoins, the gate electrodes (while being insulated from them). In other words, for each repeat unit, a single $N^+$ emitter region extends in the horizontal direction from one insulated gate electrode to the other and in the vertical direction by a distance X.

3.5 The problem posed in the description is essentially to achieve a satisfactory combination of low ON state resistance, a short circuit current which is not excessive and the prevention of the latch-up phenomenon. The Board sees no reason to doubt that an appropriate combination of these performance parameters could be achieved by the device of the present invention, nor was this called into question by the Examining Division. The issue to be decided is therefore whether, starting from the IGBT of Fig. 16 of D1, a skilled person would be motivated by the prior art to incorporate the features listed under point 3.1, above.

3.6 In the light of the contents of the three communications cited in the decision according to the state of the file, the Board's understanding of the position of the Examining Division in relation to inventive step is as follows:

Claim 1 (as then on file) differed from the closest prior art only in features (c) and (d), as listed above.

In the embodiment of Fig. 2 of document D4 the widths Wp and Wn corresponded to the claimed widths W and X. From the passage in column 10, lines 32-44 the skilled person would derive that by increasing Wp/Wn the latch-up withstand level and load short-circuit withstand level can be increased, whereas by reducing Wp/Wn the on-state resistance can be reduced. The skilled person would therefore arrive at the claimed ratio by normal design experiments.

Furthermore, in the embodiment of Figs. 42 and 43 of document D6, the widths Wn and Wp (Fig. 43) corresponded to the claimed widths X and W, and in paragraph [0031], "typical and adequate values" of Wn=12 µm and Wp=18 µm were cited.

3.7 The Board does not find these arguments entirely convincing. In D4, no numerical values for X, W or the ratio X/W are given. In D6, although the value of Wn (corresponding to X) is 12 µm, and hence within the claimed "20 µm or less", the ratio Wn/Wp (i.e. X/W) would be 12/18, i.e. 0.666, which is outside the claimed range. Thus, D6 would appear to teach away from the invention.

Moreover, in looking for suitable modifications of the closest prior art, it is questionable whether the skilled person would actually consider these embodiments, neither of which bears a particularly close structural similarity to the arrangement of Fig. 16 of D1. As one example, in Fig. 16 of D1 a p+ (emitter) layer 6 is in contact with the p-type base

layer 4; no p+ emitter layer is present in either of the cited embodiments of D4 and D6.

3.8 In any event, the Board considers that the invention (as formulated in claim 1 of auxiliary request 7) differs from the closest prior art also in the features (a), (b) and (e) listed above under point 3.4, and it must therefore also be considered whether, starting from the embodiment of Fig. 16 of D1, the skilled person would find it obvious to incorporate these features.

3.9 Within the context of claim 1, features (a), (b) and (e), in combination, define that the **surface side** of the semiconductor substrate (between the two linearly arranged insulated gate electrodes) is formed as a series of repeated units, each unit being constituted by two regions:

- a first-conductivity-type region, which itself is constituted by a first-conductivity-type [$P^+$] emitter region and a first-conductivity-type [P] (channel); and
- a second-conductivity-type [$N^+$] emitter region.

The emitter electrode contacts these regions on the surface side.

3.10 Within the context of the technical field, and in the light of the terminology of the claim itself ("parallel to the surface side of the semiconductor substrate"), it is implicit that the term "surface side of the semiconductor substrate" means a **planar** surface side.

Hence, to transform the arrangement of Fig. 16 of D1 into that defined by claim 1, at least the following steps would be required:

3.11 Firstly, the electrode 10 which extends to the bottom of the groove 210 would have to be replaced by a planar electrode contacting the semiconductor substrate on the upper side surface only, as was recognised in the communication dated 19 January 2011 (point 4.1). The Examining Division concluded that both types of electrode were known, and it would be obvious to replace one with the other "where circumstances make it desirable".

3.12 Secondly, according to claim 1, an $N^+$ emitter region extends in the horizontal direction from one insulated gate electrode to the other and in the vertical direction by a distance X (see point 3.4, above), and so in the arrangement of Fig. 16 of D1, the groove 201 in the regions adjacent the depicted n-type source layers 5 would have to be filled such that, at the surface side of the semiconductor substrate, these layers extend continuously between the insulated gates 7.

3.13 Thirdly, claim 1 specifies that in the regions between the N+ emitter regions (i.e. in a first-conductivity-type region) the surface side of the semiconductor substrate is formed as a first-conductivity-type "channel region" which faces the gate electrodes) and a first-conductivity-type [P+] emitter region. Hence, in the arrangement of Fig. 16 of D1, in the intermediate regions between n-type source layers 5, the p+ layer 6 would have to be redesigned so that it forms part of the surface side of the semiconductor substrate, and is in contact with the planar electrode.

3.14 It is clear from paragraphs [0058] and [0059] of D1 that the arrangement of Fig. 16 has been carefully designed with a view to providing "a high performance

trench insulating gate type IGBT". The steps listed above which would be required to transform this arrangement into one conforming to claim 1 of auxiliary request 7 would amount to an almost total redesign of the device. Such a transformation would be so radical that it would be difficult to regard it as an obvious measure even if some indication to proceed in this direction could be identified in the prior art. In the present case, the Board is unable to identify any such indication.

3.15 The Board therefore concludes that the subject-matter of claim 1 of auxiliary request 7 involves an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:
- claim 1 of auxiliary request 7 as filed during oral proceedings at 15.50;
- description pages 1-27 as filed during oral proceedings;
- figures 1-31 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated