Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 29 September 2016

Case Number: T 0697/12 - 3.4.03

Application Number: 06786943.8

Publication Number: 1902474

IPC: H01L29/786, H01P1/15

Language of the proceedings: EN

Title of invention:
METHOD AND APPARATUS FOR USE IN IMPROVING LINEARITY OF MOSFETS USING AN ACCUMULATED CHARGE SINK

Applicant:
PEREGRINE SEMICONDUCTOR CORPORATION

Headword:

Relevant legal provisions:
EPC Art. 52(1), 123(2)
EPC 1973 Art. 54, 56, 84

Keyword:
Novelty - (yes)
Inventive step - (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0697/12 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 29 September 2016

Appellant: (Applicant)	PEREGRINE SEMICONDUCTOR CORPORATION 9450 Carroll Park Drive San Diego, CA 92121 (US)
Representative:	Richards, John Ladas & Parry LLP Temple Chambers 3-7 Temple Avenue London EC4Y 0DA (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 18 November 2011 refusing European patent application No. 06786943.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 06 786 943 for failing to meet the requirements of the EPC for the reasons given in the communications dated 4 February 2009 and 22 July 2011.

In those communications it was stated *inter alia* that the subject-matter of claim 1 was not clear within the meaning of Article 84 EPC, was not new within the meaning of Article 54 EPC, and did not involve an inventive step within the meaning of Article 56 EPC.

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Claims 1 – 10 of the "Request 15.38" filed at 15.38 during oral proceedings;

Description pages 2 – 6, 8 - 14, 16, 18 – 24, 26 – 39, 41 – 46, 48 – 49, 51 – 52, 54, and drawings sheets 1/32 – 32/32 as published;

Description pages 1, 7, 15, 17, 25, 40, 47, 50, 53, 55, 56, 57 as filed during oral proceedings.

III. The following documents are referred to in this decision:

D1: US 2001/0015461 A1

D4: EP 1 006 584 A2

D9: J B KUO, S-C LIN: "Low-Voltage SOI CMOS VLSI Devices and Circuits" 2001, WILEY INTERSCIENCE, NEW YORK, XP001090589, pages 57-60 and 349-354

D10: US 5 959 335 A.

IV. Claim 1 reads as follows:

"A circuit comprising an SOI NMOSFET, the circuit comprising:
a) the NMOSFET (300) having a gate (302), a drain (304), a source (306), a body (312) and a charge sinking terminal (308') electrically connected to the body (312); the circuit being arranged to selectively operate the NMOSFET in an off state where, due to the gate bias, carriers having opposite polarity to the channel carriers accumulate in the channel region of the body (312) of the NMOSFET (300); and
b) a charge sinking mechanism (308) operatively coupled to the body (312) of the NMOSFET (300) via said charge sinking terminal (308');
wherein the charge sinking mechanism is provided for, when the NMOSFET is in said off state, removing said accumulated carriers by maintaining said charge sinking terminal at a bias voltage VACS that is negative with respect to both the source and drain bias voltage, wherein the charge sinking mechanism has an impedance greater than 10^6 ohms."

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 The subject-matter of claim 1 may be seen as being based on claim 1 as originally filed, with the term "accumulated charge sink (ACS)" replaced by "charge sinking mechanism" (see e.g. paragraph 101), the nature of the accumulated charge being defined at the end of paragraph a).

2.2 The deletion of "floating body" does not contravene the requirements of Article 123(2) EPC, as the MOSFET is now defined as an SOI MOSFET.

This also represents a necessary clarification of the subject-matter (Article 84 EPC 1973), as the MOSFET of the invention does not, in fact, have a floating body, but rather is of a type (an SOI MOSFET) which - in the absence of the ACS or similar counter-measures - *would have* a floating body, but as a result of coupling the body to the claimed charge sinking mechanism (ACS) the body is no longer floating and the accumulated charge is thereby removed. This is more clearly brought out by the present wording.

2.3 Further amendments and clarifications are based on the application as originally filed as follows: the invention relates to a circuit comprising an SOI MOSFET (e.g. paragraph 0021); the MOSFET is an NMOSFET (claims 4-7); the MOSFET has a gate, a drain, a source and a body (claim 2, but in any event implicit in the term "MOSFET"); the originally claimed "accumulated charge regime" refers to the operation of the MOSFET in the off state where, due to the gate bias, carriers having opposite polarity to the channel carriers accumulate in the channel region of the body (claims 2 and 3 and paragraph 0101); the charge sinking mechanism is

operatively coupled to the body of the NMOSFET via a charge sinking terminal (originally "ACS terminal", see e.g. paragraphs 099-0101); the charge sinking mechanism removes the accumulated carriers by maintaining the charge sinking terminal at a bias voltage VACS that is negative with respect to both the source and drain bias voltage (paragraphs 0101, 0105, 0133 etc.); the charge sinking mechanism has an impedance greater than 10^6 ohms (e.g. claim 23, paragraph 091).

2.4 The subject-matter of claim 1 is therefore satisfactorily based on the application as originally filed. Dependent claims 2-10 are also considered to meet the requirements of Article 123(2) EPC.

3. *Novelty in the light of document D1*

3.1 In the communications referred to in the contested decision according on the state of the file, the Examining Division concluded that the subject-matter of the independent claims as then on file lacked novelty. This finding was substantiated by a detailed analysis in relation to document D1.

3.2 Document D1 discloses a circuit (implicit: at least the biasing arrangements of the device are disclosed) comprising an SOI NMOSFET, the circuit comprising the NMOSFET having a gate, a drain, a source, and a body (claim 1; paragraphs [0110]-[0112]).

3.3 In contrast to the present invention, document D1 is mainly concerned with effects occurring when the NMOSFET is in the on state, i.e. when a positive voltage is applied to the gate electrode, so that the PN junction portion (76, 78) connecting the body region

to the gate electrode is reverse biased (see e.g. claim 1, paragraph [0118] and Fig.1).

3.4 However, as pointed out by the Examining Division, Figs. 39 and 40 disclose that a negative gate voltage (Vg) down to -1 V may be applied, which would put the NMOSFET into an off state. Furthermore, it is disclosed that the drain voltage (Vd) may be as low as 0.1 V. The source voltage (Vs) is implicitly at a reference voltage of 0 V.

Under the disclosed conditions: Vg = -1 V, Vd = 0.1 V, and Vs = 0 V, holes having opposite polarity to the channel carriers (electrons) would accumulate in the channel region of the body, as explained in paragraph 010 of the present application.

In the embodiment of Fig. 34 and paragraph [0163] a "resistance portion R" is provided, putting the gate electrode 1500 and the body region 1400 in electrical contact. Hence, in the off state defined above, the body will be at the same potential as the gate, and therefore negative with respect to both the source and drain bias voltage. As a result, the resistance portion R will remove the accumulated holes, and may properly be referred to as a "charge sinking mechanism".

3.5 In the light of the above, the following features of claim 1 are considered to be disclosed in document D1:

- *"the circuit being arranged to selectively operate the NMOSFET in an off state where, due to the gate bias, carriers having opposite polarity to the channel carriers accumulate in the channel region of the body (312) of the NMOSFET (300);*

- *"a charge sinking mechanism (308) operatively coupled to the body (312) of the NMOSFET (300) via said charge sinking terminal (308');*

- *"wherein the charge sinking mechanism is provided for, when the NMOSFET is in said off state, removing said accumulated carriers by maintaining said charge sinking terminal at a bias voltage VACS that is negative with respect to both the source and drain bias voltage".*

3.6 According to document D1, the resistance portion R may have a resistance of 50 kΩ (paragraphs [0177], [0180]). In paragraph [0185] the reference to "resistance portion R (56 k Q)" may possibly be intended to read "56 kΩ". No other values for the resistance are disclosed.

The feature that "the charge sinking mechanism has an impedance greater than 10^6 ohms" is therefore not disclosed, and hence the claimed subject-matter is novel over the disclosure of document D1.

4. *Novelty in relation to other documents*

4.1 Claim 1 now defines:

(a) *"A circuit comprising an SOI NMOSFET"* such that in the off state, the charge sinking terminal is maintained *"at a bias voltage VACS that is negative with respect to both the source and drain bias voltage"*; and that

(b) *"the charge sinking mechanism has an impedance greater than 10^6 ohms"*.

4.2 In relation to feature (a) it is noted that, for the previous versions of claim 1 which were directed to MOSFETs *per se*, the specification of the bias voltages to be applied would have been open to the objection that this related to a method of operating a MOSFET, and placed no limitation on the claimed device. In the present formulation directed to a "circuit comprising an SOI NMOSFET", the Board can accept that the definition of the (relative) bias voltages must be seen as a concrete feature implying a clear limitation on the claimed subject-matter.

4.3 Neither feature (a) nor feature (b) was present in the version of claim 1 on which the contested decision was based, or in the version filed with the statement of grounds of appeal. The Board is satisfied that none of the documents cited in the contested decision or in the communication of the Board discloses these features in combination, and hence the subject-matter of claim 1 is new within the meaning of Article 52(1) EPC and Article 54 EPC 1973.

5. *Inventive step*

5.1 In the contested decision, the analysis was based chiefly on document D1, and the Board also sees this as the most relevant document. The analysis of inventive step is therefore based on on document D1 as closest prior art.

5.2 The general aim of the present invention, as stated in claim 1, is the removal of carriers having the opposite polarity to the channel carriers which accumulate in the channel region in the off state. It was noted above under point 3.3 that while the arrangement of document D1 is mainly concerned with on state effects, an off

state is also disclosed in which the above aim would in practice be achieved.

5.3 It is therefore to be determined whether an inventive step can be acknowledged on the basis of the sole distinguishing feature of claim 1 over document D1, namely:

"the charge sinking mechanism has an impedance greater than 10^6 ohms".

5.4 The following is a summary of the analysis presented in the description of the present application in relation to this feature.

It is known to use "body contacts" or "body ties" for overcoming the problem of accumulated charge (paragraph 088 *et seq.*). In the prior art, however, such arrangements are directed towards the problems posed by accumulated charge "of the same polarity as the majority carriers of the semiconductor material under the capacitor oxide" (paragraph 010). This type of charge accumulation occurs in the on state, in which charge can accumulate very rapidly, requiring the body contact to have very low impedance. The off state charge accumulation with which the present invention is concerned occurs much more slowly, and a high impedance contact is perfectly adequate (paragraphs 090-094).

Furthermore, the arrangements for providing low impedance body connections necessarily lead to parasitic capacitances, whereas the high impedance body connection ("charge sinking mechanism") of the present invention may be positioned remotely from the source and drain, making minimal contact with the body,

thereby overcoming the problem of parasitic capacitance (paragraph 095).

5.5 The Board sees no reason to question this analysis, and hence the problem may be seen as reducing or eliminating the negative effects associated with carriers of opposite polarity to the channel carriers which accumulate in the channel region in the off state, without introducing parasitic capacitance.

5.6 In document D1 the impedance of the resistance portion R is 50 kΩ, and within the context of the disclosed arrangement, the Board can see no reason why it should be considered obvious to a skilled person to increase this value by a factor of twenty. In particular, it must be assumed that 50 kΩ has been selected as being suitable for achieving those effects in the on state with which document D1 is concerned, and the idea that the skilled person would be prepared to compromise the these effects by dramatically increasing the impedance of the resistance portion in order to achieve effects which have nothing to do with the underlying purpose of the disclosed arrangement is not plausible.

5.7 The following cited documents mention an impedance of 1 MΩ or more in relation to the body contact.

5.8 Document D4 seeks to provide low threshold voltage CMOS operation without greatly increased leakage current in the off state. This is achieved by controlling the threshold voltage by means of a bias applied to the body via a well region. Thus the technical considerations motivating the device of document D4 are entirely different to those of document D1.

Moreover, the well region resistance "is determined in consideration of the effect of a substrate current and an AC transient phenomenon" (paragraph [0052]). While the first of these considerations gives an upper limit of "not more than 10^6 ohms" (paragraph [0054]), the second implies a typical well resistance of "about 2000 Ω" (paragraph [0055]).

5.9 In document D9, in dealing with "kink" effects, resistances of 1 MΩ and greater are experimented with but found disadvantageous (page 59, first paragraph). In addition, the body contact is directly connected to the source, so that, in the off state, the charge sinking terminal is not maintained at a bias voltage that is negative with respect to both the source and drain bias voltage, as required by claim 1.

5.10 Document D10 describes an SOI CMOS device designed for enhanced avalanche multiplication of current through the device when the FET is on, and for removal of the body charge when the FET is off. This is achieved by providing a high resistance path of at least 1 MΩ coupling the body to the source. The Board is not persuaded that the skilled person would find it obvious to combine the very different teachings of documents D1 and D10.

Moreover, document D10 teaches the use of a high impedance body contact in combination with the feature that the body contact is directly connected to the source, so that in the off state, the charge sinking terminal is not maintained at a bias voltage that is negative with respect to both the source and drain bias voltage.

5.11 In the light of the above, the Board does not believe that a skilled person would be led in an obvious manner to the subject-matter of claim 1, which is therefore judged to involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   Claims 1 – 10 of the "Request 15.38" filed at 15.38 during oral proceedings;

   Description p. 2 – 6, 8 - 14, 16, 18 – 24, 26 – 39, 41 – 46, 48 – 49, 51 – 52, 54, and drawings sheets 1/32 – 32/32 as published;

   Description p. 1, 7, 15, 17, 25, 40, 47, 50, 53, 55, 56, 57 as filed during oral proceedings.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated