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Datasheet for the decision of 26 September 2017

Case Number: T 1040/12 - 3.4.03

Application Number: 07250477.2

Publication Number: 1936704

IPC: H01L33/00

Language of the proceedings: EN

Title of invention:
Semiconductor light emitting device package and method for manufacturing the same

Applicant:
LG Electronics Inc.
LG Innotek Co., Ltd.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56, 83
EPC Art. 52(1), 123(2)

Keyword:
Amendments - added subject-matter (no)
Sufficiency of disclosure - after amendment - (yes)
Inventive step - after amendment - (yes)

Decisions cited:

Catchword:

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Case Number: T 1040/12 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 26 September 2017

Appellant: (Applicant 1)	LG Electronics Inc. 20, Yoido-Dong Yongdungpo-Gu Seoul (KR)
Appellant: (Applicant 2)	LG Innotek Co., Ltd. 98, Huam-ro Jung-gu Seoul (KR)
Representative:	Zardi, Marco M. Zardi & Co. SA Via Pioda 6 6900 Lugano (CH)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 13 December 2011 refusing European patent application No. 07250477.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	W. Van der Eijk

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 07 250 477 on the ground that the subject-matter of the main request and the first to fourth auxiliary requests did not meet the requirements of Article 123(2) EPC.

II. At the end of the oral proceedings held before the Board the appellants requested that the decision under appeal be set aside and that a patent be granted in the following version:

Claims:
1-6 filed at oral proceedings before the Board at 14:00;

Description:
pages 1, 6-8 as filed by letter dated 3 August 2010,
pages 2-5, 9, 11—22 as originally filed,
pages 10, 23-29 filed at oral proceedings before the Board at 15:30;

Drawings:
sheets 1/10 -10/10 as originally filed

III. The following document cited by the Examining Division is referred to:

D2: US 2005/0121686 A1

IV. Claim 1 of the main request reads as follows

"A light emitting device package comprising:

a first substrate (200) of a ceramic material having a first surface, a second surface, and two through holes (210), and a metal or a conductive film (220) formed in each through hole (210);
a second semiconductor substrate (100) bonded to the first substrate (200), the second substrate (100) having a light emitting device mounting hole (120), and a reflection film (140) formed on a side wall surface of the mounting hole (120), wherein the second substrate (100) has a first conductivity;
two first electrodes (230) arranged on the first surface, each first electrode (230) being connected to the metal or the conductive film formed in an associated one of the through holes (210);
two second electrodes (240) arranged on the second surface, each second electrode (240) being connected to an associated one of the first electrodes (230) via the metal or conductive films in an associated one of the through holes (210);
one light emitting device (300) arranged in the mounting hole (120), and electrically connected to the first electrodes (230); and
two diffusion layers (131) each located in the second substrate (100) and extending from a surface of the second substrate (100) facing the first substrate (200) into the second substrate (100) to a depth which is less than the thickness of the second substrate (100), each of the diffusion layers (131) having a second conductivity that is opposite to the first conductivity,
wherein the two diffusion layers (131) and the second substrate (100) form two corresponding zener diodes (130),
wherein each of the two zener diodes (130) is electrically connected to the light emitting device

(300) via an associated one of the two first electrodes (230),
wherein an insulating layer is disposed between the second substrate (100) and each of the first electrodes (230), the insulating layer comprising through openings, a contact pad being provided inside of each of said through openings, each of the Zener diodes (130) being electrically connected to an associated one of the first electrodes (230) through an associated one of said contact pads."

V. In a communication under Article 15(1) RPBA the Board expressed doubts whether the subject-matter of the claims annexed to the statement of grounds of appeal met the requirements of Article Article 83 EPC 1973 and Article 123(2) EPC, and briefly discussed the comments of the Examining Division on inventive step.

VI. The present sole request differs considerably from the requests on which the contested decision was based, and so the arguments of the Examining Division substantiating its decision to refuse the application are no longer relevant and need not be repeated here.

Reasons for the Decision

1. *Article 123(2) EPC*

1.1 Claim 1 of the current request is seen as being based on independent claim 7 (or alternatively claim 18) as originally filed, now limited to the details of the "First Embodiment" (paragraphs [0046]-[0087] and Figs. 2-12 of the application as originally filed).

1.2 Several objections were raised by the Examining Division under Article 123(2) EPC against the requests then on file. In particular, the Examining Division pointed to the failure to define two substrates bonded together, the fact that certain requests defined only a single zener diode and the failure to specify that the zener diodes were formed by providing diffusion layers in a semiconductor substrate. These objections have been overcome by amendment.

The Board is therefore satisfied that the subject-matter of claim 1 meets the requirements of Article 123(2) EPC. Dependent claims 2-6 are also satisfactorily based on the original application.

2. *Article 83 EPC 1973*

2.1 In the Board's communication it was pointed out that the completed packages depicted in the figures (e.g. Fig. 10) do not - if the figures are taken at face value - represent workable arrangements. Each zener diode is shown to comprise two regions of different conductivities (a diffusion layer and a part of the second substrate), and both regions are depicted as being in physical (and presumably electrical) contact with the same first electrode (230). The zener diode would thereby be short circuited.

Something is clearly missing from these figures, and this is confirmed in paragraph [0063], according to which, after the diffusion mask (132) is removed:

"an insulating layer is deposited over the upper surface [clearly "substrate" is intended here] 100. Thereafter, a pad open process (not shown) may be

carried out, to electrically connect the zener diodes 130 to the external circuit."

2.2 Although somewhat briefly described, the appellants argued that the skilled person would understand how to carry out such an electrical connection process. This is considered plausible.

2.3 Each zener diode is thereby disclosed in paragraph [0063] as being connected to the external circuit, and this external connection is disclosed elsewhere to be via a respective first electrode, a metal or conductive film in a through hole and a second electrode (see paragraph [0076] and Fig. 10).

2.4 It is not specified in paragraph [0063] which part of the zener diode (diffusion layer side or second substrate side) is connected to the external circuit or where the insulating layer is opened. Again, the Board does not regard this as amounting to an inadequate disclosure of the invention, as the skilled person would understand that it is the diffusion layer which must be connected to the external circuit (with the second substrate being insulated from such a connection).

The only other possibilities would lead to clearly non-functional arrangements. Connecting the second substrate to the first electrode (and insulating the diffusion layer from it) would leave the diffusion layer side of the zener diode without any electrical connection. Connecting the first electrode to both the second substrate and the diffusion layer would short circuit the zener diode.

2.5 It was also pointed out by the Board in oral proceedings that even if the skilled person would find in paragraph [0063] an adequately disclosed connection arrangement, this arguably did not represent a disclosure of the claimed invention, since claim 1 as then on file seemed to point to a different connection arrangement in which the diffusion layers were located on the upper surfaces of the first electrodes, suggesting the absence of an intervening insulating layer. This objection has been overcome by amendment of claim 1.

2.6 The Board is therefore satisfied that the requirements of Article 83 EPC 1973 are met.

3. *Inventive step*

3.1 The Board agrees with the view of the appellants and the position of the Examining Division in the contested decision that Document D2 represents the closest prior art.

3.2 According to the original application, the (non-semiconductor) substrate could take the form of a PCB (see e.g. claim 2 or claim 8, as originally filed), and hence the Examining Division's identification of the claimed first substrate (200) with the PCB (31) of D2 is reasonable.

The identifications of the second substrate and the diffusion layers in claim 1 with the semiconductor substrate (14) and the n-type regions (34A, 34B), respectively, are also clearly reasonable. Consequently, the first electrodes (230) may be identified with the "external mounting pads" (26A, 26B), and the claimed mounting hole has a clear

counterpart in D2 in the form of the cavity (16), which may have a reflecting film on its side wall (D2, paragraph [0041]).

3.3 The subject-matter of claim 1 therefore differs from D2 in the following features (labels added by the Board):

(a) the first substrate is made of a ceramic material;
(b) the first substrate has two through holes, and a metal or a conductive film is formed in each through hole;
(c) the second semiconductor substrate is bonded to the first substrate;
(d) each first electrode is connected to the metal or the conductive film formed in an associated one of the through holes;
(e) two second electrodes arranged on the second surface, each second electrode being connected to an associated one of the first electrodes via the metal or conductive films in an associated one of the through holes;
(f) each of the two zener diodes is electrically connected to the light emitting device via an associated one of the two first electrodes;
(g) an insulating layer is disposed between the second substrate and each of the first electrodes, the insulating layer comprising through openings, a contact pad being provided inside of each of said through openings, each of the Zener diodes being electrically connected to an associated one of the first electrodes through an associated one of said contact pads.

3.4 According to claim 1, each of the two zener diodes is electrically connected to the light emitting device via

an associated one of the two first electrodes (feature (f)).

3.5 Hence, according to claim 1, each first electrode has three electrical connections: an external connection via the metal/conductive film in the through holes and the second electrodes, and internal connections to a respective zener diode and to the light emitting device. At each first electrode the internal circuit therefore branches into two electrically parallel pathways:

A first path is defined by the first electrodes being connected to the light emitting device to deliver electrical power to the device.

A second path, electrically parallel to the first path, is defined by the first electrodes being connected to respective zener diodes. It is implicit that these connections are to the diffusion layers (see point 2.4, above) which form zener diodes with the adjacent part of the second semiconductor substrate, the remainder of the second semiconductor substrate connecting the two zener diodes in a back to back arrangement.

3.6 Document D2 (see Fig. 2) also discloses an arrangement having an electrical path by which the light emitting device is powered in parallel with a path comprising back to back zener diodes (formed by n-type regions (34A, 34B) connected by p-type region 36 of the semiconductor substrate (14)).

3.7 However, according to claim 1, electrical power is delivered to the light emitting device via electrodes, and metallic or conductive films, and the semiconductor

regions exist only in the second path having the back to back zener diodes.

By contrast, in D2 the n-type semiconductor regions (34A, 34B) form part of the common paths, so that electrical power is delivered to the light emitting device via these semiconductor regions. The Board accepts the appellants' argument that such paths will generally have a higher resistance.

3.8 Compared with the closest prior art, the claimed invention can therefore be seen as providing electrical connections to the light emitting device which display reduced resistance, and hence reduced dissipation of power.

3.9 Adapting the arrangement of D2 to conform to claim 1 in this respect would require a significant redesign on a scale which could not be considered obvious to a skilled person, especially as the Board sees no hint or suggestion, either in D2 or in the other prior art cited in examination, which would incite the skilled person in this direction.

3.10 The Board does not find it necessary to discuss the other distinguishing features listed above, or the problems which the appellants argue that they solve, since the above considerations are sufficient for the Board to conclude that the subject-matter of claim 1 involves an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Claims:
1-6 filed at oral proceedings before the Board at 14:00;

Description:
pages 1, 6-8 as filed by letter dated 3 August 2010,
pages 2-5, 9, 11—22 as originally filed,
pages 10, 23-29 filed at oral proceedings before the Board at 15:30;

Drawings:
sheets 1/10 -10/10 as originally filed

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated