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Datasheet for the decision of 13 January 2016

Case Number: T 1943/12 - 3.5.05

Application Number: 07715572.9

Publication Number: 1994464

IPC: G06F3/14, G09G5/00

Language of the proceedings: EN

Title of invention:
INTERFACE APPARATUS AND METHOD THEREOF

Applicant:
LG Display Co., Ltd.

Headword:
Display interface/LG

Relevant legal provisions:
EPC Art. 54(2), 56

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

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Case Number: T 1943/12 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 13 January 2016

Appellant: (Applicant)	LG Display Co., Ltd. 20, Yoido-dong Youngdungpo-gu Seoul 150-721 (KR)
Representative:	Ter Meer Steinmeister & Partner Patentanwälte mbB Nymphenburger Straße 4 80335 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 March 2012 refusing European patent application No. 07715572.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	P. Cretaine
	F. Blumer

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division, posted 23 March 2012, to refuse European patent application No. 07715572.9 on the grounds of lack of inventive step (Article 56 EPC), having regard to the disclosure of

D3: "HD66790", 26 May 2004, Renesas Technology Corporation, Japan,

combined with the disclosure of

D5: "S1Dl9122 Series Technical Manual", September 2005, Seiko Epson Corporation, Japan,

with respect to a Main Request, Auxiliary Request I, and Auxiliary Request II.

Additionally, it was objected that Auxiliary Request II also did not meet the requirements of Article 84 EPC.

II. Notice of appeal was received on 21 May 2012 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was received on 1 August 2012. The appellant requested that the decision of the examining division under appeal be set aside and that a patent be granted on the basis of a Main Request or any of Auxiliary Requests I to IV filed with the statement setting out the grounds of appeal. The claims of the Main Request and of Auxiliary Requests I and II were identical to the claims of the Main request and Auxiliary Requests I and II, respectively, on which the decision was based. In addition, oral proceedings were requested as an auxiliary measure.

III. A summons to oral proceedings scheduled for 13 January 2016 was issued on 19 October 2015. In an annex to this summons, the board gave its preliminary opinion on the appeal pursuant to Article 15(1) RPBA. The board agreed with the appellant that document D5 was not prior art according to Article 54(2) EPC and that the prior art acknowledged in the description with respect to Figure 1 and paragraphs [5] to [15] of the published application might be considered as the closest prior art. Objections were raised under Article 56 EPC with respect to all the requests on file, having regard to the above-mentioned closest prior art and to the disclosure of

D1: "MOS INTEGRATED CIRCUIT µPD1618O1" April 2003, NEC Electronics Corporation, Japan.

IV. With a letter dated 11 December 2015, the appellant objected that Figure 1 of the application was not prior art according to Article 54(2) EPC. He filed Auxiliary Request Ia, to be considered before Auxiliary Request I, Auxiliary Request IIa, to be considered before Auxiliary Request II, and Auxiliary request V.

V. Oral proceedings were held as scheduled on 13 January 2016. During the proceedings the appellant filed amended pages 2b and 2c of the description. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of any of the Main Request, Auxiliary Request Ia, Auxiliary Request I, Auxiliary Request IIa, Auxiliary Request II, Auxiliary Request III, Auxiliary Request IV and Auxiliary Request V, the Main Request, Auxiliary Requests I, II, III and IV as filed with the statement

setting out the grounds of appeal, Auxiliary Requests Ia, IIa and V as filed with letter dated 11 December 2015. At the end of the oral proceedings, the board announced its decision.

VI. Claim 1 of the **Main Request** reads as follows :

"An interface apparatus (120) comprising:
- a signal synthesizer (121) for outputting display signals constituting pixels of a display module (130), display control signals for controlling the display signals to be displayed on the display module (130) and chip control signals for controlling a chip provided to the display module (130), wherein the display signals include R, G and B signals transmitted in parallel, wherein the chip control signals include a chip select signal (CS), a serial clock signal (SCK), and a serial data input signal (SDI), wherein the display control signals include a horizontal synchronized input signal (Hsync), a vertical synchronized input signal (Vsync), a data enable signal (DE) and a data clock signal (DCLK);
- a connecting means (122) for connecting the signal synthesizer (121) and a signal separator (123) including first transmission lines connected with the signal synthesizer (121) and for sequentially transmitting the chip control signals and the display signals by the same transmission lines under the control of the data enable signal (DE), and second transmission lines for transmitting the display control signals; and
- the signal separator (123) for separating the display signals and chip control signals from the first transmission lines,
wherein the signal synthesizer (121) outputs the chip control signals to the first transmission lines for a

first period where a data enable signal (DE) included in the display control signals is disabled, and outputs the display signals to the first transmission lines for a second period where the data enable signal (DE) is enabled".

The main request comprises a further independent claim for a corresponding interface method (claim 2).

Considering the outcome of the decision, the details of the auxiliary requests do not need to be considered.

Reasons for the Decision

1. The appeal is admissible.

2. Prior art

2.1 Document **D5** is a version of a technical manual for specific LCD driver ICs of Seiko Epson Corporation, the document being marked "Preliminary Confidential" on every other page, in particular on the most relevant pages 29 and 33. This represents a strong indication that a person could not have gained knowledge of it without a breach of confidentiality, and that the document was provided for internal use at EPSON only. This is corroborated by the fact that the manual version is designated as Rev.0.9b, a number which strongly indicates that this version was not intended for public availability.

The board therefore judges that document **D5** was not available to the public before the priority date of the present application and is thus not prior art according to Article 54(2) EPC.

2.2 **D3** discloses a source driver for display signals. Pins are provided for receiving display control signals Vsync, Hsync, DOTCLK, ENABLE, display signals PD17-0 data, and chip control signals CS, SCL and SDI from a CPU (see in particular Figures 1 and 23). Pages 53 to 55 (see in particular Figure 12) further show that the RGB display signals are transmitted via the pins PD17-0 when the ENABLE SIGNAL is not constantly high, i.e. enabled, but not during the front porch and back porch of the Vsync signal, during which the enable signal is constantly high, i.e. disabled. D3 does not disclose that command signals, in particular the chip control signals, and display signals may be transmitted within the interface by the same parallel transmission lines in time division.

2.3 **D1** discloses a TFT-LCD source driver circuit including a display RAM. The circuit comprises an interface to a CPU (see page 2) for receiving RGB display signals, display control signals (Hsync, Vsync, DOTCLK) and chip control signals (CS, SI, SCL), each signal being received on a different pin of the circuit. Signals D0 to D17 are received on a single bus pin of the I/0 BUFFER and represent, depending on the value of an RS signal, either data signals or command signals (see pages 13 and 22).

2.4 The appellant had argued in the statement setting out the grounds of appeal that the apparatus as disclosed in Figure 1 of the application was a better starting point for assessing inventiveness (see section 3.1 of the statement setting out the grounds of appeal). However, during the oral proceedings, the appellant pointed out that the apparatus shown in Figure 1 was only an unpublished internal background art of the

inventor. Figure 1 therefore cannot be considered as prior art according to Article 54(2) EPC.

3. Main Request

D1 could be considered as the closest prior art to the subject-matter of claim 1 since it discloses a circuit wherein command and display signals may be entered on the same input pins.

The circuit of D1 (see Figure 1) receives input data (D0-D17, RGB00-RGB25) and a plurality of control signals (/CS, RS, SI, SCL, HSYNC, VSYNC) via separate pins. The data on pins D0-D17 is written into the display RAM and from there converted into analogue data and output to the data lines of the display panel via pins Y1-Y240. Therefore D1 only describes a combined timing controller and signal converter, as shown in the application in Figure 1, reference sign 14 or in Figure 3, reference sign 131. A synthesizer 121 and a separator 123, as defined in claim 1, are not directly identifiable in Figure 1 of D1.

Any interface feature which could correspond to an interface feature of claim 1 would thus be between the input pins of the circuit of D1 and the I/O buffer of D1. D1 describes (see page 1, "Features") that the circuit may have three different selectable interfaces to the CPU. The RGB interface can be used only to overwrite the display data RAM. The 8-bit serial interface can, as such, not transmit RGB signals, as well as chip control signals, in parallel. Therefore the only interface which the skilled person could consider is the i80/M68 CPU parallel interface, which is further described as being used for writing both the display data RAM and registers. The appellant plausibly

argued that, as could be seen in Figure 1 of D1, the display signals (RGB) are transmitted via different lines than the display control signals (HSYNC, VSYNC,DOTCLK) and the chip control signals (SI, SCL): the display signals are transmitted in parallel via the Data register to the Display data RAM, whereas the control signals are transmitted to the Command decoder, the Address decoder or via the RGB controller to the RGB shift register.

The skilled person would not get any hint from D1 to modify the above-mentioned interface for transmitting chip control signals sequentially on the same lines as display signals, with the aim of minimizing the number of transmission lines. Although it is stated in D1 (see pages 13, 30, and 41) that signals D0 to D17 are received on a single bus pin of the I/O buffer and represent, depending on the value of the RS signal, either data signals or command signals, nothing is disclosed in D1 about the origin, content, and transmission target of these data signals, as well as about the separation of data and command signals. The link between RGB display signals and chip control signals on one side and the above-mentioned data and command signals on the other side is thus not obvious. Moreover, the circuit of D1 requires at least three control signals, namely /CS, /WR, and RS for setting and controlling the interface, whereas claim 1 only requires the DE signal.

Neither would the skilled person get any hint from D3. In that respect the board agrees with the decision under appeal (see Reasons 1.1.1 on page 5), that D3 does not disclose sequentially transmitting the chip control signals and the display signals by the

same transmission lines under the control of the data enable signal, separating the display signals and chip control signals from the same parallel transmission lines, and outputting the chip control signals to the transmission lines for a first period where a data enable signal included in the display control signals is disabled.

For these reasons the board judges that the subject-matter of claim 1 involves an inventive step, having regard to the prior art on file (Article 56 EPC).

4. Since the appellant's main request is allowable, there is no need for the board to consider the auxiliary requests.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following documents:
   - Claims 1 and 2, filed as Main Request with the statement setting out the grounds of appeal;
   - Description:
     - pages 1 and 4 to 6 of the International application as published,
     - pages 2 and 3 as filed with letter dated 30 August 2010,

- page 2a as filed with letter dated 2 November 2011,
- pages 2b and 2c as filed during the oral proceedings before the board on 13 January 2016;

- Drawing sheets 1/2 and 2/2 of the International application as published.

The Registrar: The Chair:

L. Malécot-Grob A. Ritzka

Decision electronically authenticated