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Case Number: T 2258/12 - 3.4.03

Application Number: 09161629.2

Publication Number: 2136354

IPC: G09G3/36

Language of the proceedings: EN

Title of invention:
Display device, liquid crystal display device and electronic device including the same

Applicant:
Semiconductor Energy Laboratory Co, Ltd.

Headword:

Relevant legal provisions:
EPC Art. 52(1), 123(2)
EPC 1973 Art. 56

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

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Case Number: T 2258/12 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 14 July 2016

Appellant: (Applicant)	Semiconductor Energy Laboratory Co, Ltd. 398, Hase Atsugi-shi, Kanagawa 243-0036 (JP)
Representative:	Grünecker Patent- und Rechtsanwälte PartG mbB Leopoldstraße 4 80802 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 31 May 2012 refusing European patent application No. 09161629.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 09 161 629 on the grounds that the subject-matter of the main request did not meet the requirements of Article 123(2) EPC, Article 52(1) in combination with Article 54(1) and (2) EPC, and Article 52(1) in combination with Article 56 EPC, and that the subject-matter of the auxiliary request did not meet the requirements of Articles 84 and 123(2) EPC, and Article 52(1) in combination with Article 56 EPC.

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Description:
Pages 1, 9-16,19, 21-23, 25-32, 34-72, 74-76, 78-80, 82-85 as originally filed,
Pages 3, 8, 17, 18, 20, 24, 33, 73, 77, 81, 86 as filed during the oral proceedings before the Board,
(originally filed pages 4-7 being deleted),
Pages 2, 2a, 2b filed with letter dated 8 February 2012;

Claims: 1-4 of the main request as filed during the oral proceedings before the Board (in clean copy at 14.20 hours);

Drawings: Sheets 1/16 to 16/16 as originally filed.

III. The following documents cited by the Examining Division are referred to in this decision:

D1: US 2007/0070008 A1

D2: Invited Paper: The Worlds Largest (82-in.) TFT-LCD; SANG SOO KIM; 2005 SID INTERNATIONAL SYMPOSIUM; pages 1842-1847, XP007012410.

IV. Claim 1 of the main and sole request submitted during oral proceedings reads as follows:

"A display device comprising:

a plurality of pixels, wherein each pixel (502; 605) is divided into first to nth, n is a natural number of 2 or more, subpixels (502_1 to 502_n; 606a; 606b), wherein each of the first to nth subpixels (502_1 to 502_n; 606a; 606b) is provided with an electrode for driving a liquid crystal element;

n wiring groups (112_1 to 112_n) each supplying M, where M is a natural number of 2 or more, different voltages;

a plurality of first wiring groups (111), wherein a digital signal with N, where N is a natural number of 2 or more, bits is input into each said first wiring group (111);

a plurality of scanning lines (Gi);

a plurality of converter portions (100);

each converter portion (100) having a function to convert the respective digital signal into a first to nth analog signal, the converter portion (100) including first to nth circuits (101_1 to 101_n) each

being connected to a respective wiring group (112_1 to 112_n) and having a function of:

converting the digital signal into an analog signal by using the M different voltages supplied from a respective wiring group (112_1 to 112_n), and

inputting the analog signal to the respective one of the first to nth subpixels (502_1 to 502_n; 606a; 606b) through the respective one of a first to nth wiring (113_1 to 113_n);

wherein each of the first to nth circuits (101_1 to 101_n) are connected to the respective first to nth wirings (113_1 to 113_n), the respective first to nth wirings being connected to respective first to nth subpixels (502_1 to 502_n; 606a; 606b);

wherein the first to nth subpixels (502_1 to 502_n; 606a; 606b) of each pixel are connected to a same scanning line (Gi);

the display device further comprising a signal line driver circuit (601) adapted to write each of the first to nth analog signals into a respective one of the first to nth subpixels (502_1 to 502_n; 606a; 606b) during one gate selecting period, wherein the signal line driver circuit comprises the plurality of converter portions;

wherein the first to nth wiring (113_1,..., 113_n) are part of the display device."

Independent claim 2 of the main and sole request submitted during oral proceedings reads as follows:

"A display device comprising:

a plurality of pixels, wherein each pixel (502; 605) is divided into first to nth, n is a natural number of 2 or more, subpixels (502_1 to 502_n; 606a; 606b), wherein each of the first to nth subpixels (502_1 to 502_n; 606a; 606b) is provided with an electrode for driving a liquid crystal element;

n wiring groups (112_1 to 112_n) each supplying M, where M is a natural number of 2 or more, different voltages;

a plurality of first wiring groups (111), wherein a digital signal with N, where N is a natural number of 2 or more, bits is input into each said first wiring group (111);

a plurality of scanning lines (Gi);

a plurality of converter portions (100);

each converter portion (100) having a function to convert a respective digital signal into a first to nth analog signal and including a decoder circuit (201), wherein the decoder circuit has the function to decode the digital signal with N bits into a further digital signal with M bits,

each converter portion (100) including first to nth circuits (101_1 to 101_n) each being connected to a respective wiring group (112_1 to 112_n) and having a function of:

converting the further digital signal into an analog signal by using the M different voltages supplied from a respective wiring group (112_1 to 112_n), and

inputting the analog signal to the respective one of the first to nth subpixels (502_1 to 502_n; 606a; 606b) through the respective one of a first to nth wiring (113_1 to 113_n);

wherein each of the first to nth circuits (101_1 to 101_n) are connected to the respective first to nth wirings (113_1 to 113_n), the respective first to nth wirings being connected to respective first to nth subpixels (502_1 to 502_n; 606a; 606b);

wherein the first to nth subpixels (502_1 to 502_n; 606a; 606b) of each pixel are connected to a same scanning line (Gi);

the display device further comprising a signal line driver circuit (601) adapted to write each of the first to nth analog signals into a respective one of the first to nth subpixels (502_1 to 502_n; 606a; 606b) during one gate selecting period, wherein the signal line driver circuit comprises the plurality of converter portions;

wherein the first to nth wiring (113_1,..., 113_n) are part of the display device."

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (Article 123(2) EPC)*

2.1 As stated by the appellant, claim 1 is based on claim 3 as filed, incorporating features of the display device depicted in Fig. 11A (and described in the associated passages of the description), and further incorporating a digital-analog converter portion 100 of the type depicted in Fig. 1C (and described in the associated passages of the description). The specific objection raised in the Board's communication pursuant to Article 15(1) RPBA has been overcome by amendment.

2.2 Independent claim 2 differs in that the digital-analog converter portion 100 is of the type depicted in Figs. 2A, 2B, 3, 4A, 4B etc. (and described in the associated passages of the description).

2.3 The Board is satisfied that the claimed subject-matter meets the requirements of Article 123(2) EPC.

3. Inventive Step starting from document D2

3.1 In the opinion of the Board, the most suitable starting point is the display described in section 4 and depicted in Figs. 12 and 13(b) of document D2. In this "double data line design", each of the corresponding A and B subpixels has its own dedicated data line (e.g. R1(A), R1(B)), and the subpixels of a given pixel share a common gate line, e.g. Gn.

The display device of claim 1 of the main request appears to differ chiefly in the converter portion 100. The arrangement in claim 1 essentially corresponds to a conventional analog R-string (resistor string) gamma correction procedure (see, for example, paragraphs

[0114], [0282]-[0288] of the present description, and Figs. 9B, 9C).

On the other hand, the gamma correction of section 4 of document D2 is shown in Fig. 12 to occur at the stage of the left and right source boards. Although not explicitly stated in document D2, the input to and the output from the source boards both appear to be digital, implying that digital gamma correction is employed.

3.2 Thus, in relation to the embodiment of section 4, document D2 does not disclose, even implicitly, the following features:

(a) *n* wiring groups (112_1 to 112_n) each supplying M different voltages (M is a natural number of 2 or more);

(b) the converter portion including first to nth circuits each being connected to a respective wiring group (112_1 to 112_n) and having a function of:

(c) converting the digital signal into an analog signal by using M different voltages supplied from a respective wiring group (112_1 to 112_n), and

(d) wherein each of the first to nth circuits (101_1 to 101_n) are connected to the respective first to nth wirings (113_1 to 113_n).

3.3 As mentioned above, these differences essentially define that analog rather than digital gamma correction is employed. Digital gamma correction uses look-up tables, which, driven at the required high speeds,

generate heat and increase power consumption (description, paragraphs [0007] and [0008]), and the appellant's formulation of the objective problem - reducing power consumption and heat generation - appears plausible.

3.4 The general principles of gamma correction or switching for S-PVA pixels is described in a separate part of document D2 (page 1844, paragraph bridging left-hand and right-hand columns, and Fig. 7), according to which "there are two approaches toward optimal gamma (γ) control, namely analog γ switching and digital γ switching", and the "basic difference is in which domain [i.e. analog or digital] the input data is changed".

Fig. 7(a) shows analog γ-voltage switching using "two different sets of R-string networks" and Fig. 7(b) shows digital γ-voltage switching using lookup tables (LUT-A and LUT-B).

Document D2 does not attempt a full evaluation of the relative merits of these two approaches, and in particular does not mention aspects such as power consumption and heat generation. Thus, on the basis of the problem posed in the application, document D2 does not provide any explicit incentive for the skilled person to implement analog γ-voltage generation in the arrangement of section 4.

3.5 On the other hand, the Board is of the opinion that both analog and digital generation of γ-voltages, including the use of R-strings and lookup tables, were commonly known at the priority date of the present application, and it also appears to be accepted in the application that "resistor string DACs" are well-known,

as they are mentioned in paragraph [0114] without further explanation.

The skilled person would therefore be familiar with both of the approaches to generating γ-voltages shown in Figs. 7(a) and 7(b) of document D2, and with their respective strengths and weaknesses. On this basis, it could be argued that the selection of one or the other approach represents the sort of choice between two well-known alternatives which is generally not considered to involve an inventive step.

3.6 However, even if, *arguendo*, it would be an obvious possibility for the skilled person to modify the arrangement of section 4 of document D2 by implementing analog γ-correction, the question remains whether this would lead to the claimed subject-matter.

As mentioned above, Fig. 12 appears to relate entirely to digital data processing, and since analog γ-correction results in an analog output, the skilled person would not consider implementing it within the circuit arrangement schematically depicted in block form in this figure. If analog γ-correction were to be incorporated, it would have to take place after the arrangement of Fig. 12, for example at the column driver stage, as in document D1 (see e.g. Figs. 3 and 4).

3.7 The input to any analog γ-correction circuit for the A subpixel would therefore be the original pixel data, re-formatted into S-PVA data using the A data look-up table (page 1845, paragraph right-hand column, first paragraph of section 4), and subjected to further processing (DCC etc.). The input to any analog γ-correction circuit for the B subpixel would be the

original pixel data, re-formatted into S-PVA data using the B data look-up table, and subjected to similar further processing. Since the point of providing separate A and B data look-up tables is that they are different from each other, it follows that the digital signals input into the analog γ-correction circuits for the A and B subpixels would be different.

According to claim 1, however, the converter portion includes first to nth circuits, each having a function of "converting **the digital signal** into an analog signal ... and inputting the analog signal to the respective one of the first to nth subpixels" (emphasis added by the Board), the digital signal referred to being the previously introduced digital signal with N bits which is input into each first wiring group (111). It is thus the **same** digital signal which is input into each of the first to nth circuits.

3.8 Hence, even if the possibility of applying analog γ-correction to the arrangement of section 4 of document D2 occurred to the skilled person, implementing it would not lead to the subject-matter of claim 1.

3.9 According to independent claim 2, it is not the original digital signal with N bits which is input into the first to nth circuits, but a decoded "further digital signal with M bits". Nevertheless, it is still the same digital signal which is input into each of the first to nth circuits, and hence the skilled person would not arrive at the subject-matter of claim 2 in an obvious manner for the reasons mentioned in connection with claim 1.

4. *Inventive step starting from document D1*

4.1 Both claim 1 and claim 2 define a display device comprising a plurality of pixels, wherein each pixel "is divided into first to *n*th ... subpixels". In the opinion of the Board, the formulation "is divided into" (as opposed to e.g. "comprises" or "has"), must be interpreted as meaning that each pixel has precisely n subpixels; no more, no less.

Claims 1 and 2 also define "a plurality of scanning lines ... wherein the first to nth subpixels ... of each pixel are connected to a same scanning line". Consequently, the independent claims define that all of the subpixels of each pixel are connected to the same scanning (i.e. gate) line.

4.2 In document D1, the colour pixels (see e.g. Fig. 1) comprise three colour areas (R, G, B), each further divided into high and low grey scale areas (VH, VL). Each pixel is addressed by two scanning (gate) lines (GL1, GL2), with line GL1 connected to areas RVL, GVH and BVL, and line GL2 connected to areas RVH, GVL and BVH. The resulting "staggered arrangement" appears to be a fundamental part of the teaching of document D1 (see e.g. abstract, claim 1), and it is not apparent how it could be easily modified to one in which all of the subpixels of each pixel are connected to the same gate line, or indeed why a skilled person would wish to do this.

Hence, on the basis of this difference alone, the Board concludes that a skilled person would not arrive at the subject-matter of either claim 1 or claim 2 in an obvious manner starting from document D1, and it is not necessary to investigate whether there are further non-obvious differences.

5. In the light of the foregoing considerations, the Board judges that the subject-matter of claims 1 and 2 involves an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

   Description:
   Pages 1, 9-16,19, 21-23, 25-32, 34-72, 74-76, 78-80, 82-85 as originally filed,
   Pages 3, 8, 17, 18, 20, 24, 33, 73, 77, 81, 86 as filed during the oral proceedings before the Board,
   Pages 2, 2a, 2b filed with letter dated 8 February 2012,

   Claims: 1-4 of the main request as filed during the oral proceedings before the Board in clean copy at 14.20 hours,

   Drawings: Sheets 1/16 to 16/16 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated