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Datasheet for the decision of 20 October 2017

Case Number: T 0232/13 - 3.4.03

Application Number: 09172487.2

Publication Number: 2180518

IPC: H01L29/786, H01L21/336

Language of the proceedings: EN

Title of invention:
Method for manufacturing semiconductor device

Applicant:
Semiconductor Energy Laboratory Co, Ltd.

Headword:

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
Amendments - added subject-matter (no) - after amendment
Inventive step - (yes) - after amendment

Decisions cited:
T 0482/92

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It can be changed at any time and without notice.

Catchword:

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Case Number: T 0232/13 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 20 October 2017

Appellant: (Applicant)	Semiconductor Energy Laboratory Co, Ltd. 398, Hase, Atsugi-shi, Kanagawa, 243-0036 (JP)
Representative:	Grünecker Patent- und Rechtsanwälte PartG mbB Leopoldstraße 4 80802 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 July 2012 refusing European patent application No. 09172487.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Papastefanou
	C. Schmidt

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing the European patent application No. 09 172 487.2 (published as EP 2 180 518 A2). The Examining Division found that claim 1 of the Main request and claim 1 of each of the First and Third Auxiliary requests before it did not meet the requirements of Article 123(2) EPC. In addition, claim 1 of the Main request as well as claim 1 of each of the First, Second and Third Auxiliary requests did not involve an inventive step within the meaning of Article 56 EPC.

II. The following documents were cited in the appealed decision:
D1: US 2008/176364 A1
D2: EP 1 933 293 A1
D3: US 2006/0110867 A1

III. In a communication pursuant to Rule 100(2) EPC, the Board indicated that the sole request filed with the grounds of appeal met the requirements of Article 52(1) EPC but it raised objections under Article 84 EPC because the description was not adapted to the claims and the prior art documents D1, D2 and D3 were not cited therein.

IV. In reaction to this communication by the Board, the Applicant (Appellant) filed an amended description taking into account the Board's objections.

V. The Appellant requests that the decision under appeal be set aside and that a patent be granted based on the following application documents:

- Claims: 1-3 filed with the grounds of appeal;
- Description: Pages 1-71 filed with letter dated 11 September 2017;
- Drawings: Sheets 1-30 as originally filed.

VI. Independent claim 1 of the sole request has the following wording:

A method for manufacturing a semiconductor device, comprising:

forming a gate electrode layer over a substrate having an insulating surface;

stacking a gate insulating layer, a first oxide semiconductor film, a second oxide semiconductor film for a source region and a drain region, and a conductive film over the gate electrode layer;

forming a first mask layer over the gate insulating layer, the first oxide semiconductor film, the second oxide semiconductor film, and the conductive film;

performing a first etching with the first mask layer to etch the first oxide semiconductor film, the second oxide semiconductor film, and the conductive film so that a first oxide semiconductor layer, a second oxide semiconductor layer, and a conductive layer are formed;

forming a second mask layer by ashing the first mask layer; and

performing a second etching with the second mask layer to etch the first oxide semiconductor layer, the second oxide semiconductor layer, and the conductive layer so that an oxide semiconductor layer having a depression,

a source region, a drain region, a source electrode layer, and a drain electrode layer are formed, wherein the first mask layer is formed using a light-exposure mask,

wherein the gate insulating layer includes a silicon oxynitride film,

wherein each of the first etching and the second etching is dry etching with use of an etching gas including chlorine and oxygen,

wherein the oxide semiconductor layer having the depression includes a region with a smaller thickness than a region overlapping the source region or the drain region; and

wherein the second oxide semiconductor film is thinner and has a higher conductivity than the first oxide semiconductor film.

Reasons for the Decision

1. The appeal is admissible.

2. The sole request on file is based on the Main request which forms the basis of the appealed decision.

3. Amendments (Article 123(2) EPC)

3.1 Claim 1 is based on original claim 6.

3.2 The Examining Division, making reference to paragraph [0018] of the original description, found that the definition of the second oxide semiconductor film being thinner and having a higher conductivity than the first

oxide semiconductor film without the specification that it (the second oxide semiconductor film) is used for the source region and the drain region was an unallowable intermediate generalisation.

The omitted feature has been added to claim 1 and this objection has been, thus, overcome.

3.3 Further amendments carried out with respect to the claim 1 which formed the basis of the appealed decision are:

- the feature that *the gate insulating layer includes a silicon oxynitride film* was added; support for this amendment can be found paragraph [0037] of the description as originally filed;
- the features that *the etching gas includes chlorine and oxygen* were added; these features come from claims 2 and 3 of the refused request and find support in original claims 8 and 9 respectively.

3.4 Dependent claims 2 and 3 correspond to original claims 10 and 11 respectively.

3.5 The Board is satisfied that the requirements of Article 123(2) EPC are met.

4. Inventive Step (Article 56 EPC)

4.1 The Examining Division (see point 2.2 of the appealed decision) considered document D1 to be the closest prior art and found that, since D1 did not disclose a semiconductor device with a second oxide semiconductor film, the features differentiating claim 1 before it from D1 were:

- the semiconductor device having a second oxide semiconductor film,
- which was thinner and had a higher conductivity than the first oxide semiconductor film.

4.2 Compared to claim 1 before the Examining Division, current claim 1 has the additional features:

- the gate insulating layer includes a silicon oxynitride film;
- the etching gas used in the first and second dry etching includes chlorine and oxygen.

These features are not disclosed in D1, either.

4.3 According to the established case law of the Boards of Appeal, the closest prior art for assessing inventive step is normally a prior art document disclosing subject-matter conceived for the same purpose as the claimed invention and having the most relevant technical features in common (T 482/92, Reasons, point 4.1, third paragraph).

4.4 In view of the distinguishing features between Claim 1 and D1 identified above, the Board considers document D2 to be more suitable as closest prior art. D2 also describes a method of manufacturing a semiconductor device (see Figure 3) with a first (1014 in Figure 3) and a second (1015) oxide semiconductor film. The second oxide semiconductor film has a higher conductivity (e. g. paragraph [0100]) than the first one. In some embodiments the gate insulating layer includes silicon oxynitride (e.g. paragraphs [0089], [0166], [0169], [0225]).

A first mask layer (e. g. resist 1016 in Figure 3) is formed using a light exposure mask (paragraph [0052])

used for a first etching (paragraph [0053]). This first mask layer is then ashed to form a second mask layer (paragraph [0056]) which is then used for a second etching (paragraph [0058]) to form an oxide semiconductor layer having a depression, a source region, a drain region, a source electrode layer and a drain electrode layer (see Figures 6 and 7).

Except for the first embodiment, in all other embodiments in D2 the second oxide semiconductor film is thicker than the first (paragraphs [0092], [0115]-[0116], [0170]-[0171]). In the first embodiment the two oxide semiconductor films are of the same thickness (paragraph [0051]). Regarding the etching, in all embodiments the oxide semiconductor films are etched by wet etching (paragraphs [0053] and [0058], [0093], [0120], [0179]).

4.5 Hence, the method in claim 1 differs from the one in D2 in that:

- the first and second etchings performed to the first and second oxide semiconductor films are dry etchings using an etching gas including chlorine and oxygen; and
- the second oxide semiconductor film is thinner than the first.

4.6 There is no apparent synergy between these features and it would appear legitimate to assess them separately with respect to inventive step. This is also the least favourable approach for the Appellant.

4.6.1 As explained in paragraph [0066] of the present application, when dry etching using a gas including chlorine and oxygen is performed on In-Ga-Zn-O based semiconductor films, and in the case of using a silicon

oxynitride film as gate insulating layer, the selectivity ratio of the first and second oxide semiconductor films with respect to the gate insulating layer can be increased,thus, limiting the damage to the gate insulating layer.

4.6.2 In D2 there is no dry etching performed on the oxide semiconductor films at all. Moreover, as described in paragraph [0179], when the oxide semiconductor films are of the same materials as in the present application, improved selective properties are obtained in combination with the etching solutions used. Even if it were considered that dry etching was generally known to the skilled person (it is also disclosed in D1 see paragraphs [0037]-[0041]), the technical effect obtained by the use of dry etching in the claimed method is also obtained in D2 but with wet etching and the use of appropriate etching solutions. There appears to be no motivation for the skilled person starting from D2 to use dry etching instead of wet etching since the identified technical problem is already solved in D2, albeit in a different way.

Even if the technical problem to be solved is formulated more generally as how to find an alternative way to obtain the same technical effect (better selectivity properties for the oxide semiconductor films), the skilled person would not arrive at the solution to use dry etching with the specific combination of gases (chlorine and oxygen) in an obvious way, since there is nothing in the prior art documents that would point him towards this direction. In D1, the proposed dry etching is performed using Fluorine-based gas containing Argon (Ar) or Helium (He), see paragraph [0038]. In D3 there is mention of

dry etching used only for forming the gate terminal and a CF_4+Ar etching gas is mentioned (paragraph [0420]).

Hence, the Board concludes that this feature is not obvious.

4.6.3 Regarding the feature of the second oxide semiconductor film being thinner than the first, the Board notes that in D2 the thickness values of the two oxide semiconductor films are explicitly stated in all embodiments. Except from the first embodiment where the thickness of the two films has the same value (150 nm - paragraph [0051]), in all other embodiments, the second oxide semiconductor film is thicker than the first (150 nm and 100 nm respectively - paragraphs [0092], [0115]-[0116], [0170]-[0171]). Hence, in D2 the possibility to have the second oxide semiconductor layer thinner than the first is explicitly excluded.

4.6.4 Even if it were considered that this feature of the claim does not address any particular technical problem, the skilled person starting from D2, where it is explicitly excluded that the second oxide semiconductor layer can be thinner than the first, would not be incited to implement this feature in any obvious way.

4.7 The conclusion is that the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC 1973.

5. The description has been adapted to the claims and prior art documents D1-D3 are mentioned therein (paragraph [0004]).

6. The Board is, hence, satisfied that the application meets the requirements of the EPC.

Order

For these reasons it is decided that:

1. The appealed decision is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   - Claims: 1-3 filed with the grounds of appeal;
   - Description: pages 1-71 filed with letter dated 11 September 2017;
   - Drawings: Sheets 1-30 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated