Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 23 February 2018

Case Number: T 0421/13 - 3.5.02

Application Number: 07789925.0

Publication Number: 2145391

IPC: H03M13/03, H04L1/00

Language of the proceedings: EN

Title of invention:
Integrated Circuit Comprising Error Correction Logic, and a Method of Error Correction

Applicant:
NXP USA, Inc.

Relevant legal provisions:
EPC Art. 56, 84

Keyword:
Inventive step - (no)
Claims - clarity (no)

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 0421/13 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 23 February 2018

Appellant: (Applicant)	NXP USA, Inc. 6501 William Cannon Drive West Austin TX 78735 (US)
Representative:	NXP Semiconductors, 134 avenue du Général Eisenhower BP 72329 31023 Toulouse Cedex 1 (FR)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 November 2012 refusing European patent application No. 07789925.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Lord
Members:	H. Bronold
	J. Hoppe

Summary of Facts and Submissions

I. The appeal lies from the decision of the Examining Division to refuse European patent application No. 07789925.0 for lack of clarity (Article 84 EPC) and lack of inventive step (Article 56 EPC).

II. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request or, if that was not possible, that a patent be granted on the basis of the claims of one of the first to fourth auxiliary requests, all filed with the notice of appeal. Together with their statement setting out the grounds of appeal, the appellant requested reimbursement of the appeal fee.

III. In a first communication the board informed the appellant that it had doubts whether the invention claimed in the main request and in the first to fourth auxiliary requests was sufficiently disclosed in the sense of Article 83 EPC.

IV. The appellant replied with letter dated 18 September 2014 and filed six further documents in support of their argumentation. They provided arguments why it was possible to calculate Reed-Solomon-syndromes (RS-syndromes) in an iterative manner without the full Reed-Solomon-codeword (RS-codeword).

V. In a second communication sent together with the summons to attend oral proceedings, the board informed the appellant *inter alia* that although it accepted that iterative calculation of RS-syndromes was possible, there were no features in the claims reflecting such

iterative calculation. Further, there seemed to be no corresponding disclosure in the application. The application did not provide a complete technical teaching for the first embodiment, or for the second embodiment. Thus, not withstanding the requirements of Article 84 EPC, the subject-matter of all requests seemed to lack an inventive step in the sense of Article 56 EPC.

VI. With fax dated 22 February 2018 the appellant informed the board that they did not intend to attend the oral proceedings scheduled for 23 February 2018. No further requests or arguments were brought forward.

VII. Oral proceedings before the board took place on 23 February 2018 in the absence of the appellant.

VIII. Claim 1 of the main request reads as follows:

"An integrated circuit comprising a memory (560, 760) and forward error correction, FEC, decoder logic (320) coupled to said memory, said FEC decoder logic arranged to receive data, comprising application data, from a host application process (308), to perform error detection upon the received data, and to generate error correction information for application data in which errors are detected;
which FEC decoder logic (320) comprises or is operably coupled to logic arranged to transmit error free application data out of said application data back to the host application process (308);
wherein the integrated circuit is characterised in that it has option (a) or (b):

option (a) being:
the FEC decoder logic is arranged:

to store in the memory (560) out of said application data only application data in which errors are detected,
to perform error correction upon the application data stored in the memory (560), and
to transmit corrected application data back to the host application process (308);

option (b) being:
the FEC decoder logic (320) is adapted:
to send both the error free application data and the application data in which errors are detected back to the host application process without storing in said memory (760),
to generate error correction information in the form of an error correction patch enabling the host application process to correct any detected errors itself, and to transmit the error correction patch to the host application process (308)."

Options (a) and (b) concern the first and second embodiments of the invention, respectively.

Independent claim 15 of the main request relates to a corresponding method.

IX. The claims of the first to fourth auxiliary requests relate to more limited versions of options (a) and/or (b) as defined in claim 1 of the main request. In the second auxiliary request, option (a) is deleted. In the third auxiliary request, a section building logic and an error detection logic are added to option (b) while option (a) is still deleted. The fourth request is directed to both options (a) and (b) in combination with the section building logic and the error detection logic.

Compared to the main request and the second to fourth auxiliary requests, which are all directed to an integrated circuit, the independent apparatus claim of the first auxiliary request is directed to an apparatus comprising means to execute a host application process, the apparatus comprising options (a) or (b) and in the case of option (a) said means comprising a further memory for storing error-free application data.

All auxiliary requests include independent method claims corresponding to the respective independent apparatus claims.

X. The arguments of the appellant, as far as they are relevant for this decision, can be summarised as follows:

The appellant in their reply dated 18 September 2014 argued that calculation of RS-syndromes was possible iteratively on incomplete RS-codewords and column-wise instead of row-wise. They referred *inter alia* to document D5, "R&D White Paper WHP 031" on "Reed-Solomon error correction" by C.K.P. Clarke, dated July 2002, in particular to the application of Horner's method to RS-syndrome calculation described on page 16 of that document.

Further, according to the first embodiment of the invention, all 64 syndromes of each row were updated with values from the currently received section, wherein updated meant changed and not discarded. Likewise for the second embodiment, upon reception of an MPE-FEC section, syndrome information was updated. In both the first and the second embodiments all

syndromes were stored, not just those of incorrect application data.

In addition, the application did not seek to address a reduction of the memory size of an MPE-FEC decoder. The application was directed to relaxation of memory requirements instead. Therefore, it was not necessary to reflect the reduction of the memory size by introducing respective features in the independent claims.

Moreover, the contested decision was not reasoned, contrary to the requirements of Rule 111(2) EPC and the appellant's right to be heard according to Article 113(1) EPC had been violated. Therefore, it was equitable to reimburse the appeal fee.

The appellant did not present any arguments concerning the objections under Article 84 EPC and Article 56 EPC raised by the board in its second communication under Article 15(1) RPBA sent together with the summons to oral proceedings.

Reasons for the Decision

1. The appeal is admissible.

2. Clarity and inventive step (Articles 84 and 56 EPC)

2.1 The present application concerns multi protocol encapsulated - forward error correction (MPE-FEC) which

is used for receiving digital video broadcasts on mobile devices.

Taking into account the arguments and documents brought forward by the appellant in their reply dated 18 September 2014, based in particular on document D5 and the arguments concerning Horner's method, the board accepts that iterative calculation of RS-syndromes is possible even without the full RS-codeword in the context of MPE-FEC decoder circuits.

2.2 The appellant further argues that the technical problem solved by the invention would be a relaxation of memory requirements instead of a reduction of the memory size, when compared to a standard MPE-FEC decoder storing an entire MPE-FEC frame.

The board does not agree with this interpretation. The context of the passages cited by the appellant on page 3, line 24 and page 8, line 25 of the description as originally filed is clearly a reduction of the memory size, since both passages aim at a reduction of the size of the integrated circuit which is in this context equivalent to the reduction of the size of the memory.

The board therefore understands that the technical problem which the application seeks to solve is to reduce the size of the memory in a MPE-FEC decoder, and that in order to provide a solution to this technical problem, the known principle of iterative calculation of RS-syndromes needs to be applied and adapted to the technical context. Specifically, the use of a technique such as Horner's method means that only those data values being used in a particular iteration need to be stored in the decoder memory, in contrast to prior art methods which need to store entire rows of data.

2.3 In order to comply with the requirements of Article 84 EPC and Article 56 EPC, features corresponding to this principle need to be defined in the claims.

As this is not the case the claims are unclear. Essential features of the alleged invention are missing, and their subject-matter lacks an inventive step, because it does not give rise to the technical effect which the invention is alleged to provide.

Consequently, already for this reason, the application complies neither with Article 84 EPC nor with Article 56 EPC.

2.4 Having regard to the subject-matter claimed in the main request and the first to fourth auxiliary requests, the board considers further steps beyond the known iterative calculation of RS-syndromes to be necessary in order to arrive at a technical teaching that might be patentable, in the sense that the steps would need to be defined in the claims if the technical effect of reducing memory size is to be taken into account for the assessment of inventive step over a standard MPE-FEC decoder storing at least one entire MPE-FEC frame.

With the current subject-matter claimed and described such a technical effect is neither mentioned nor achieved. For example, for the first embodiment there is no disclosure of how the alleged column-wise calculation and updating of all 64 syndromes is carried out. It is pure speculation how received sections of MPE-data are processed into the 64 syndromes of a MPE-row. The corresponding description of the first embodiment on page 6, lines 25 to 32, merely defines

the result, namely that all 64 syndromes for each row are updated with values of the current section.

Regarding the second embodiment, it is defined on page 9, lines 30 to 33 that "The CRC [cyclic redundancy check] computation logic 720 ... generates syndromes for the MPE data ... and updates syndrome information stored in ... FEC memory 760". A standard CRC computation logic would only provide CRC-syndromes regarding the current section. How an otherwise unspecified (i.e. standard CRC) computation logic should calculate and update RS-syndromes of MPE-data, is not disclosed.

2.5 Thus, the application does not provide a complete technical teaching for either the first embodiment or for the second embodiment concerning the technical effect which according to the appellant underlies the alleged invention. Consequently, the claims of all requests, being technically incomplete in the same respect, do not comply with Article 84 EPC

For the same reason, the subject-matter of all requests also lacks an inventive step in the sense of Article 56 EPC over the prior art represented by the standard MPE-FEC decoder as already cited by the examining division.

2.6 Consequently, the board has arrived at the conclusion, that none of the requests on file is allowable.

Therefore, the appeal has to be dismissed.

3. Reimbursement of the appeal fee (Rule 103(1)(a) EPC)

3.1 In section 5 of the statement setting out the grounds of appeal the appellant requested reimbursement of the appeal fee "in view of the numerous violations of art. 113 and Rule 111 EPC".

3.2 According to Rule 103(1)(a) EPC the appeal fee shall be reimbursed where the Board of Appeal deems an appeal to be allowable, if such reimbursement is equitable by reason of a substantial procedural violation.

Since the board does not consider the appeal to be allowable, it would go beyond the power of the board to examine the question of whether the reimbursement of the appeal fee is equitable by reason of a substantial procedural violation.

3.3 Thus, the request for reimbursement of the appeal fee has to be refused.

Order

For these reasons it is decided that:

1. The appeal is dismissed.

2. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

U. Bultmann R. Lord

Decision electronically authenticated