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Datasheet for the decision of 11 November 2019

Case Number: T 0961/13 - 3.5.07

Application Number: 09167223.8

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Title of invention:
Memory module with reduced access granularity

Applicant:
Rambus Inc.

Headword:
Memory module with reduced access granularity/RAMBUS

Relevant legal provisions:
EPC Art. 56, 76(1), 84, 123(2)

Keyword:
Amendments - added subject-matter (no)
Inventive step - after amendment - (yes)
Remittal to the department of first instance

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Case Number: T 0961/13 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 11 November 2019

Appellant: (Applicant)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ Speiser Patentanwälte Rechtsanwälte PartGmbB Johannes-Brahms-Platz 1 20355 Hamburg (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 14 November 2012 refusing European patent application No. 09167223.8 pursuant to Article 97(2) EPC**

Composition of the Board:

Chairman	R. Moufang
Members:	P. San-Bento Furtado
	C. Barel-Faucheux

Summary of Facts and Submissions

I. The appeal lies from the decision of the Examining Division to refuse European patent application No. 09167223.8, which was filed as a divisional of European patent application No. 07782931.5. The decision under appeal cited several prior-art documents, including the following:
D3: US 2004/0256638 A1, published on 23 December 2004;
D4: US 2004/0105292 A1, published on 3 June 2004 and
D6: EP 0 910 091 A2, published on 21 April 1999.

The Examining Division decided that the subject-matter of claim 1 of the main request and of each of auxiliary requests I to IV lacked inventive step (Articles 52(1) and 56 EPC) over document D3, and that claim 1 of the main request and of auxiliary requests I and II added subject-matter beyond the content of the application as originally filed (Article 123(2) EPC). An auxiliary request V, which had been erroneously numbered as auxiliary request IV and filed four days before the scheduled oral proceedings, was not admitted into the proceedings under Rules 116(1) and 137(3) EPC. The subject-matter of claim 1 of this request was considered to lack inventive step.

The Examining Division further expressed the opinion that the features of claims 2 to 6 and 9 to 18 of the main request were obvious or known from documents D3, D4 or D6, and that none of those claims appeared to meet the requirements of the EPC with respect to inventive step. The subject-matter of claims 7 and 8 of the main request were not disclosed in the cited prior art.

II. In the statement of grounds of appeal, the appellant requested that the decision be set aside and that a patent be granted on the basis of the main request or of one of auxiliary requests I to V filed with the grounds of appeal.

III. In a communication accompanying a summons to oral proceedings, the Board expressed concerns that claim 1 of the main request did not fulfil the requirements of clarity, support by the description and basis in the application and parent application as originally filed. Similar objections applied to claim 1 of each of auxiliary requests I to V. The subject-matter of claim 1 of the main request and auxiliary requests I to V did not seem to be novel over document D3. Even when interpreting claim 1 of the main request in the light of the description, its subject-matter did not seem to be inventive.

IV. With a letter of reply the appellant filed new auxiliary requests IIIa, IVa, Va, IIIb, IVb, Vb, IIIc, IVc and Vc. Claim 1 of each of auxiliary requests IIIb, IVb and Vb was based in part on features taken from claims 7 and 8 of the main request considered by the decision under appeal.

V. Oral proceedings were held on 19 November 2018. During the oral proceedings the Board informed the appellant that auxiliary request IIIb appeared to overcome the objections of lack of inventive step but that it was doubtful whether requests IIIb, IVb and Vb complied with the requirements of Articles 76(1), 84 and 123(2) EPC. The appellant submitted a new request "Auxiliary request I new" based on auxiliary request IIIb. The Board was still not convinced that this request overcame the objections under

Articles 76(1) and 84 EPC and, due to the complexity of the case, agreed to continue the proceedings in writing in order to give the appellant one last opportunity to file an allowable amended request based on auxiliary request "I new", which related to embodiments described in paragraphs [0014] to [0018] and Figures 5A to 5E. At the end of the oral proceedings, the chairman announced that the proceedings would be continued in writing. In the oral proceedings and corresponding minutes and in a further communication, the Board informed the appellant about the type of amendments expected and said that it intended to decide the case without further oral proceedings.

VI. In a letter of reply, the appellant filed new requests called "New Main Request" and "New Auxiliary Request I". It requested that the decision of the Examining Division be set aside and that a patent be granted on the basis of the new main request or new auxiliary request I. It requested oral proceedings if the Board did not consider either of the new requests allowable.

VII. In a communication, the Board informed the appellant that it was still not convinced that the requests fulfilled the requirements of Articles 76(1) and 84 EPC, and invited the appellant to amend the claims in order to overcome the objections raised in the communication.

VIII. In its reply dated 14 August 2019, the appellant submitted new claims according to a main request and an auxiliary request I, and resubmitted the previous main request and auxiliary request I as further auxiliary requests II and III.

IX. In a telephone conversation, the Board informed the appellant that the features defined at the end of claim 1 of the new main request and auxiliary request I still added subject-matter (Article 76(1) EPC).

X. In its reply dated 23 September 2019, the appellant filed an amended set of claims as auxiliary request Ia, maintained "all previously filed request [sic]" as "higher ranking requests" and explained that the appellant was "prepared to withdraw [the] higher ranking requests once it becomes clear that the Board of Appeal [is] prepared to grant the patent on the basis of the claims in accordance with auxiliary request Ia". It again requested oral proceedings in case the Board did not consider "any of the claim sets in accordance with auxiliary request Ia or one of the previously filed requests to be allowable".

XI. In a communication, the Board expressed its opinion that it was not clear which requests were on file and invited the appellant to submit a clear formulation of its final requests.

XII. In a letter dated 15 October 2019, the appellant filed a set of claims 1 and 2 according to a main request, the claims corresponding to those of previous auxiliary request Ia, and requested remittal of the case to the department of first instance "with the order to grant a patent on the basis of the attached claims". It expressed the opinion that the remaining requests seemed irrelevant, but maintained, as auxiliary requests, the request for oral proceedings and "the earlier main and auxiliary requests".

XIII. The appellant's main final request is therefore that the contested decision be set aside and that a patent

be granted on the basis of the main request filed with the letter of 15 October 2019.

XIV. Claim 1 of the main request reads as follows:

"A memory module (300), comprising:
a first set of memory devices (301);
a second set of memory devices (303);
an interface for a single chip-select line (CS) coupled to the first set of memory devices (301) and to the second set of memory devices (303);
an interface for a command/address path (CA) coupled to the first set of memory devices (301) and the second set of memory devices (303);
an interface for a clock line (CLK) coupled to the first set of memory devices (301) and the second set of memory devices (303);
an interface for a data path (DQ) with a first component path (DQ-A) of a first width coupled to the first set of memory devices (301) and a second component path (DQB) of a second width coupled to the second set of memory devices (303), the interface for the data path (DQ) having a third width; wherein

each memory device of the first set of memory devices (301) comprises
first signal receiver circuits, and
a first sampling-latency control circuit (315) to control command/address sampling latencies, wherein the first sampling-latency control circuit (315) comprises a first configuration register (317) and a first multiplexer (321),
a first sampling-latency value (318) is programmed within the first configuration register (317) to select either an incoming chip-select signal (316) or a two-cycle delayed instance of the chip-select signal (320) to be output from the first multiplexer (321) as a

first sample-enable signal (SE(A)), wherein the chip-select signal is present on the chip-select line;
the first sample-enable signal (SE(A)) enables the first signal receiver circuits to sample row activation and column access commands (ACT, RD) present on the command/address path, wherein
each memory device of the second set of memory devices (301) comprises
second signal receiver circuits, and
a second sampling-latency control circuit (315) to control command/address sampling latencies, wherein the second sampling-latency control circuit (315) comprises a second configuration register (317) and a second multiplexer (321),
a second sampling-latency value (318) is programmed within the second configuration register (317) to select either the incoming chip-select signal (316) or the two-cycle delayed instance of the chip-select signal (320) to be output from the second multiplexer (321) as a second sample-enable signal (SE(B)), wherein the chip-select signal is present on the chip-select line;
the second sample-enable signal (SE(B)) enables the second signal receiver circuits to sample row activation and column access commands (ACT, RD) present on the command/address path, wherein
the memory module (300), being adapted to use the first and second sampling latency control circuits to operate the first set of memory devices and the second set of memory devices to access memory, where memory access can be initiated through activation of the chip-select line interpreted as simultaneously directed to both the first set of memory devices and the second set of memory devices to concurrently process data for transfer via the first data path (DQ-A) and the second

data path (DQ-B) using the third width, and memory access can be initiated through an activation of the chip-select line interpreted as directed to exactly one of the first set of memory devices (301) or the second set of memory devices (303) to process data for transfer via the respective first component path (DQ-A) or the second component path (DQ-B) at a given instant in time."

XV. Claim 2 of the main request reads as follows:

"The memory module (300) of claim 1, where each of the first set of memory devices (301) and the second set of memory devices (303) are discrete memory devices."

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

The invention

2. The present application concerns a memory system enabling efficient use of signalling resources and reduced memory access granularity (see paragraph [0005] of the published application).

2.1 According to the description, core access time improvements in dynamic random access memories (DRAMs) continue to be outpaced by signalling rate advances. In order to solve that, memory devices and subsystems output ever larger amounts of data per access in order to meet peak data transfer rates. In many cases, such as in the prior-art memory system described in paragraph [0002] with reference to Figures 1A to 1C of the application, that "is achieved through simple

extension of the output burst length; the number of data transmissions executed in succession to output data retrieved from a given location within the memory core" (paragraph [0002]). However, the extended burst length and resulting increased access granularity results in unneeded data being retrieved and transmitted, wasting power and increasing thermal load. Besides, it prevents memory access commands from being transmitted back-to-back (i.e., in successive pairs of clock cycles), thus resulting in periods of non-use on the command/address path (paragraph [0003]).

2.2 The invention addresses these problems by coupling each of two or more memory-device sets on a memory module to a respective portion of a data path and supporting independent access to each memory-device set, also called "memory sub-rank", through a shared command/address path, where the two or more reduced-granularity memory transactions are carried out concurrently, i.e. at least partly overlapping in time (paragraphs [0005] and [0007]).

2.3 In the embodiment of Figures 5A, 5B and 5E, the chip-select line is shared among the memory sub-ranks.

In order to enable independent memory commands to be received within each of the memory sub-ranks, the embodiment of Figures 5A, 5B and 5E establishes a different delay interval between chip-select line activation and sampling of the command/address paths ("sampling latency") in each of the sub-ranks so that command path sampling occurs at different times within the sub-ranks (paragraphs [0014], [0015] and [0018]).

Added subject-matter and clarity

3. Claim 1 is based on the embodiment described in paragraphs [0014], [0015] and [0018] and Figures 5A, 5B and 5E, in combination with paragraph [0024] of the application and parent application as filed.

The objections of lack of clarity and added subject-matter of the decision under appeal and those raised by the Board were overcome by amendment.

3.1 In particular, claim 1 no longer defines the features objected to in the decision under appeal and now specifies that the path CA is a command/address path coupled to the first and second set of memory devices (paragraph [0014], Figure 5A), the interface for a clock line (CLK) is coupled to the first and second sets of memory devices (paragraph [0014], Figure 5A), the "incoming chip-select signal (316)" is present on the single chip-select line (paragraph [0015], Figure 5B), and the row activation and column access commands (ACT, RD) are present on the command/address path (paragraph [0015] and Figure 5E).

3.2 Furthermore, the definition of the memory accesses has been amended in accordance with the disclosure of paragraph [0015] in combination with paragraph [0024].

3.3 The feature of claim 2 is disclosed in paragraph [0025].

4. The Board is therefore satisfied that the claims fulfil the requirements of Articles 76(1), 84 and 123(2) EPC.

Inventive step

5. Document D3 concerns a memory system which includes one or more semiconductor memory devices coupled to a

configurable-width buffer device having a bypass circuit (abstract, paragraph [0045]).

5.1 The configurable-width buffer device is positioned between or with at least one integrated circuit memory device on a substrate surface of the memory module (abstract). As illustrated in Figures 4A and 4B, the memory system of document D3 includes buffer device 405 and a plurality of memory devices 410a-410h communicating over a pair of channels 415a and 415b. Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM) (paragraphs [0072] and [0073]). Control lines (RQ) may transport control information (e.g. read, write, precharge) and address information (e.g. row and column) contained in packets (paragraph [0074]).

The configurable-width buffer device has a maximum buffer device interface width equivalent to the number of data pins or contacts provided on the buffer device's package or interface. Using the techniques described in document D3, the configurable-width buffer device may be programmed or configured to operate at interface widths and memory-device access widths other than these maximum values (paragraph [0098]).

In the embodiment described in paragraph [0146] with reference to Figure 5F of document D3, a configurable-width buffered module 660, which corresponds to a memory system as shown in Figures 3A to 3C, or 4A to 4C, includes two memory cells in corresponding memory devices and supports two modes of operation. In a first mode of operation, both memory cells are accessed. In a second mode of operation, one memory cell is accessed.

According to paragraphs [0115] and [0147] of document D3, accessing a subset of secondary channel

signal lines per transaction, or activating subsets of the available memory devices, has the benefit of reducing power consumption.

5.2 Document D3 therefore discloses a memory module directed to the same purpose as the present invention of supporting memory access with reduced granularity.

However, the memory module of document D3 does not include first and second sampling-latency control circuits to control command/address sampling latencies, wherein each of the first and second sampling-latency control circuits comprises a configuration register and a multiplexer, and wherein a first and second sampling-latency value is programmed within the respective configuration register to select either an incoming chip-select signal or a two-cycle delayed instance of the chip-select signal to be output from the respective multiplexer as a first or second sample-enable signal. Consequently, it does not disclose either that the memory module is adapted to use the first and second sampling-latency control circuits to operate the first set and second sets of memory devices to access memory in the way described in claim 1.

5.3 The claimed subject-matter therefore solves the problem of finding an alternative solution to supporting memory access with reduced granularity.

5.4 None of the cited prior-art documents discloses a sampling-latency control circuit used for the same purpose as the present invention. The Board is not persuaded either that it would be obvious for the skilled person, without a pointer in that direction, to arrive at the distinguishing features. No such pointer is found in the prior art cited in the present case.

5.5 Therefore, claim 1 fulfils the requirements of Articles 52(1) and 56 EPC. Consequently, dependent claim 2 also complies with Articles 52(1) and 56 EPC.

Conclusion

6. The claims of the main request satisfy the requirements of the EPC, but the description and drawings have not been adapted yet. The case is therefore to be remitted for grant on the basis of the claims of the main request and a description and drawings to be adapted.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the claims of the main request filed by letter of 15 October 2019 and a description and drawings to be adapted thereto.

The Registrar: The Chairman:

I. Aperribay R. Moufang

Decision electronically authenticated