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Datasheet for the decision of 11 November 2019

Case Number: T 1795/13 - 3.5.02

Application Number: 09748606.2

Publication Number: 2342820

IPC: H03F3/45

Language of the proceedings: EN

Title of invention:
Self auto-calibration of analog circuits in a mixed signal integrated circuit device

Applicant:
Microchip Technology Incorporated

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - main request (yes)

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Case Number: T 1795/13 - 3.5.02

D E C I S I O N
of Technical Board of Appeal 3.5.02
of 11 November 2019

Appellant: (Applicant)	Microchip Technology Incorporated 2355 West Chandler Boulevard Chandler, AZ 85224-6199 (US)
Representative:	sgb europe Lechnerstraße 25a 82067 Ebenhausen (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 8 April 2013 refusing European patent application No. 09748606.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	R. Lord
Members:	C. Vassoille
	R. Cramer

Summary of Facts and Submissions

I. The applicant (appellant) filed an appeal against the decision of the examining division to refuse European patent application no. 09 748 606.2, which is based on the international application published under the PCT as WO 2010/062547 A1.

II. In the decision under appeal, the examining division, setting out their grounds, came essentially to the conclusion that the subject-matter of the claim 1 as well as that of the independent claim 10 did not involve an inventive step in the sense of Article 56 EPC.

III. The following documents are relevant for the present decision:

D1: WO 02/27943 A2
D2: US 6,034,569

IV. With the statement setting out the grounds of appeal, the appellant submitted a new set of claims 1 to 15.

V. In a communication pursuant to Rule 100(2) EPC dated 2 October 2018 the board informed the appellant of its preliminary opinion that claim 1 did not seem to fulfil the requirements of Article 123(2) EPC and that the subject-matter of claim 1 further seemed not to involve an inventive step in the sense of Article 56 EPC.

VI. With letter of 1 February 2019 the appellant submitted a new set of claims 1 to 15.

VII. In a further communication pursuant to Rule 100(2) EPC dated 21 March 2019 the board informed the appellant

that the subject-matter of claims 1 and 10 seemed to involve an inventive step in view of documents D1 and D2 but that some of the dependent claims were, however, considered to contain formal defects and unallowable amendments in the sense of Article 123(2) EPC.

VIII. With letter of 22 July 2019, the appellant filed new claims 1 to 14 according to the main request and further filed an auxiliary request comprising claims 1 to 11 as well as amended description pages 1 to 10.

IX. In a further communication pursuant to Rule 100(2) EPC dated 8 August 2019 the board informed the appellant of some further remaining defects and an unallowable amendment in the sense of Article 123(2) EPC.

X. With letter of 23 September 2019, the appellant filed new claims 1 to 14 according to the main request and an amended auxiliary request comprising claims 1 to 11 as well as amended description pages 2 to 5.

XI. The board understands that the appellant's main request is that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: nos. 1 to 14 of the main request filed with letter of 23 September 2019;
Description: pages 1 and 6 to 10, submitted with letter dated 22 July 2019; pages 2 to 5 submitted with letter dated 23 September 2019;
Drawings: sheets 1/4 to 4/4 as originally filed.

XII. Claim 1 of the main request reads as follows:

"An integrated circuit comprising:

at least one analog input device (202) having a digitally controlled input offset voltage compensation circuit comprising a volatile trim register (310); and

an auto-calibration circuit, said auto-calibration circuit being coupled to said at least one analog input device (202) and to the input offset voltage compensation circuit, wherein an input offset voltage is minimized in said at least one analog input device (202) during an auto-calibration cycle,

characterized in that said auto-calibration circuit comprises a first trigger input receiving an output signal from a power on reset circuit (130) and a second trigger input (Acal) operable to be set under program control, wherein upon a power on reset, the power on reset circuit (130) is configured to initiate the auto-calibration cycle and wherein the power on reset circuit (130) is further configured to receive an output signal from a parity detection circuit (308, 312) coupled with said volatile trim register (310) wherein a parity error during operation of the at least one analog input device (202) causes a power on reset thereby initiating the auto-calibration cycle."

Claims 2 to 9 are dependent on claim 1.

XIII. Independent method claim 10 of the main request reads as follows:

"A method for minimizing an input offset voltage in an analog input device (202) having a digitally controlled input offset voltage compensation circuit arranged within an integrated circuit and comprising a volatile

trim register (310), said method comprising the steps of:

(a) monitoring a first input (A_{CAL}) of an automatic calibration circuit (300) for detecting a user invoked auto-calibration and monitoring a second input for detecting an occurrence of a power-on reset within said integrated circuit, wherein an auto-calibration cycle is initiated through either said first or second input, wherein a power on reset is further caused by a parity error in said volatile trim register (310) during operation of the at least one analog input device (202);

(b) upon initiating said auto-calibration cycle switching the analog input device(202) from a normal mode to an auto-calibration mode;

(c) minimizing an input offset voltage in said at least one analog input device (202); and

(d) switching the analog input device (202) from the calibration mode to the normal mode."

Claims 11 to 14 are dependent on claim 10.

In view of the board's decision on the main request, it is not necessary to reproduce the auxiliary request.

XIV. The appellant's arguments as far as they are relevant for the present decision were as follows:

The object of the present invention was to provide a reliable initiation of an auto-calibration cycle. To this end, the integrated circuit according to claim 1 provided for a parity error detection circuit that could cause a power on reset which further caused a re-

calibration when a parity error occurs during normal operation of the device. In this respect, the specification particularly stated the following:

> "If a parity error occurs (during normal operation of the operational amplifier 202), a power-on-reset from the POR 130 is forced and a new auto-calibration cycle takes place. This is important because the trim contents may be stored in volatile (memory), and the trim data contained therein may be corrupted during a power glitch." (see the original description on page 8, line 29 to page 9, line 2)

None of the cited prior art documents either disclosed or suggested such a mechanism. For example, document Dl neither disclosed nor suggested any type of parity control let alone that a parity error caused a reset and therefore a re-calibration instead of an immediate initiation of the auto-calibration cycle.

While document D2 may disclose that different events could initiate an auto-calibration cycle, this document however, taught that every parameter change caused a direct control of the initiation of auto-calibration. Thus, D2 taught away from the claimed solution that provided for a power-on reset when a parity error occurred.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request - inventive step (Article 56 EPC)*

2.1 Document D1 is considered to be the closest prior art. This document is concerned with an integrated circuit (see figure 1, abstract, page 10, lines 21 to 24) comprising at least one analog input device (see figure 2: 202, figure 3: 202a) having a digitally controlled input offset voltage compensation circuit (see figure 3: 302a) comprising a volatile trim register (see page 7, line 3; page 10, lines 8 to 10); and an auto-calibration circuit (figure 2: 206, figure 3: 312, 206), said auto-calibration circuit being coupled to said at least one analog input device (via comparator 204) and to the input offset voltage compensation circuit (see figure 3: 302a), wherein an input offset voltage is minimized (see the abstract, page 6, line 30) in the at least one analog input device during an auto-calibration cycle.

2.2 The subject-matter of claim 1 therefore differs from document D1 at least in that the auto-calibration circuit comprises a first trigger input receiving an output signal from a power on reset circuit, wherein upon a power on reset, the power on reset circuit is configured to initiate the auto-calibration cycle and wherein the power on reset circuit is further configured to receive an output signal from a parity detection circuit coupled with said volatile trim register wherein a parity error during operation of the at least one analog input device causes a power on reset thereby initiating the auto-calibration cycle.

2.3 According to the original description on page 8, line 29 to page 9, line 2, the trim data stored in a volatile memory may be corrupted during a power glitch. A corresponding parity error during normal operation of the operational amplifier, which may result from checking the trim register contents, consequently forces a power-on-reset and thus, an auto-calibration cycle, according to the present invention.

2.4 The objective technical problem may therefore be considered to be that of how to provide a reliable initiation of an auto-calibration cycle, as has been proposed by the appellant.

2.5 Document D1 in particular on page 9, lines 18 to 19 discloses the initiation of a calibration process, when operating parameters have changed ("The aforementioned calibration process may be periodically repeated when an operating parameter(s) may have changed").

Furthermore, document D1 on page 4, lines 26 to 27 discloses the ability of the calibration circuit to "dynamically calibrate the analog input device on demand and during operation thereof over all operating conditions". Operating conditions are mentioned in D1 to be temperature, voltage, current, speed, power, pressure, humidity, etc. (see D1 on page 2, lines 28 to 29).

Consequently, as has been outlined under point 2.2, the board agrees with the appellant that document D1 neither discloses nor suggests a power on reset to thereby initiate an auto-calibration cycle upon detection of a parity error in the volatile trim register.

2.6 Document D2 discloses an integrated circuit according to the preamble of claim 1, comprising a plurality of trigger inputs to initiate a calibration process based on a detected change in system conditions (see D2 in column 3, lines 48 to 50 and 60 to 65; column 4, lines 6 to 11) and on a periodic basis (column 2, lines 52 to 54).

However, document D2 neither discloses nor suggests a power on reset to thereby initiate an auto-calibration cycle upon detection of a parity error in the volatile trim register, as has been argued by the appellant. The board agrees with the appellant on this point.

2.7 The board therefore comes to the conclusion that the subject-matter of claim 1 is not rendered obvious by either of documents D1 or D2 or a combination thereof. The same applies to the subject-matter of independent method claim 10.

3. Conclusion

3.1 Since the subject-matter of the independent claims 1 and 10 of the main request involves an inventive step in the sense of Article 56 EPC and since the application fulfils the further requirements of the EPC, the board had to concede to the appellant's request to set the decision under appeal aside.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Claims: nos. 1 to 14 of the main request, filed with letter dated 23 September 2019

Description: pages 1 and 6 to 10, submitted with letter dated 22 July 2019, pages 2 to 5 submitted with letter dated 23 September 2019;

Drawings: sheets 1/4 to 4/4 as originally filed.

The Registrar: The Chairman:

U. Bultmann R. Lord

Decision electronically authenticated