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Datasheet for the decision of 31 January 2019

Case Number: T 2259/13 - 3.5.04

Application Number: 08726425.5

Publication Number: 2118762

IPC: H04N5/335, H04N5/217

Language of the proceedings: EN

Title of invention:
APPARATUS AND METHOD FOR STABILIZING IMAGE SENSOR BLACK LEVEL

Applicant:
JVC KENWOOD Corporation

Headword:

Relevant legal provisions:
EPC Art. 84

Keyword:
Claims - clarity (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 2259/13 - 3.5.04

D E C I S I O N
of Technical Board of Appeal 3.5.04
of 31 January 2019

Appellant: (Applicant)	JVC KENWOOD Corporation 3-12, Moriyacho Kanagawa-ku Yokohama-shi, Kanagawa 221-0022 (JP)
Representative:	Barker Brettell LLP 100 Hagley Road Edgbaston Birmingham B16 8QQ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 19 June 2013 refusing European patent application No. 08726425.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	C. Kunzelmann
Members:	M. Paci
	G. Decker

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing European patent application No. 08 726 425.5, published as international patent application WO 2008/112104 A1.

II. The decision under appeal was based on the ground that claims 1 and 4 according to the sole request then on file did not meet the requirement of clarity of Article 84 EPC.

III. With the statement of grounds of appeal, the appellant filed two sets of amended claims according to first and second auxiliary requests. The appellant also filed a clean copy of the claims underlying the decision under appeal which were maintained as its main request.

IV. The board issued a summons to oral proceedings, followed by a communication under Article 15(1) of the Rules of Procedure of the Boards of Appeal (RPBA, OJ EPO 2007, 536) in which it gave its preliminary opinion that claims 1 and 4 according to each of the main and first and second auxiliary requests did not meet the requirement of clarity of Article 84 EPC.

V. The appellant did not comment on the board's objections. Instead, in a letter dated 11 January 2019, it informed the board that it would not be attending the oral proceedings.

VI. The board held oral proceedings on 31 January 2019. As announced, the duly summoned appellant did not attend.

At the oral proceedings, the chairman noted that the appellant had requested that the decision under appeal

be set aside and that a European patent be granted on the basis of the claims according to the main request or the first or second auxiliary requests, all requests filed with the statement of grounds of appeal, or that the case be remitted to the department of first instance for further prosecution.

At the end of the oral proceedings, the chairman announced the board's decision.

VII. Claims 1 and 4 according to the appellant's **main request** read as follows:

"1. A signal processing circuit (100) for processing an output signal from a pixel array (11), the pixel array (11) having optical black pixels and active clear pixels, wherein the pixel array (11) has lines of only optical black pixels, and lines containing both optical black pixels and active clear pixels, the circuit (100) comprising:

a differential programmable gain amplifier (210), one input of the differential programmable gain amplifier (210) connected to the pixel array output signal from the pixel array (11);

an analog-to-digital converter (220) connected to the differential programmable gain amplifier (210), wherein the analog-to-digital converter (220) converts (220) a programmable gain amplifier output signal from the programmable gain amplifier (210) into a digitized output signal;

a first summing block (310) connected to an output of the analog-to-digital converter (220);

a black clamp processing block (500) connected to the summing block (310), wherein the black clamp processing block (500) compares the digitized output signal with a black reference value, and outputs a

black level adjustment signal to an input of the programmable gain amplifier (210);

a line noise correction processing block (400) connected to a second summing block (410), wherein the line noise correction processing block calculates (400) a line noise average value for black pixels in the output signal on a line-by-line basis for lines containing both optical black pixels and active clear pixels and calculates a line noise offset based on a difference between the line noise average value and the black reference value; and

a column noise correction processing block (300), wherein the column noise correction processing block (300) calculates a column noise offset for black pixels from all optical black lines in the digitized output signal, the column noise offset calculated on a column basis by calculating a difference between the digitized output signal for each black pixel and the line noise average value calculated by the line noise correction processing block (400),

wherein the first summing block (310) is configured to add the column noise offset to the clear pixels in the digitized output signal; and

the second summing block (410) is configured to add the line noise offset to the clear pixels in the digitized output signal."

"4. A method performed by the signal processing circuit (100) of claim 1 to process the output signal from the pixel array (11), the method comprising:

the black clamp processing block (500) calculating the black level adjustment signal by calculating a difference between the digitized output signal from the pixel array and the black reference value;

the line noise correction processing block (400) calculating the line noise correction value by

calculating a line noise average value from black pixel values in the digitized output signal on a line-by-line basis for lines comprising both optical black and active clear pixels;

the line noise correction processing block (400) calculating a difference between the line noise average value and the black reference value;

the column noise correction processing block (300) calculating the column noise correction value by calculating a difference between the digitized output signal for each black pixel and the line noise average value;

the black clamp processing block (500) adjusting a black level in the output signal according to the black level adjustment signal to form a second output signal;

the first summing block (310) adding the column noise correction value to the second output signal to form a third output signal;

the second summing block (410) adding the line noise correction value to the third output signal, to form a fourth output signal; and

outputting the fourth output signal."

VIII. Claims 1 and 4 according to the appellant's **first auxiliary request** read as follows (additions to claims 1 and 4 of the **main request** are underlined, deletions are ~~struck-through~~):

"1. A signal processing circuit (100) for processing an output signal from a pixel array (11), the pixel array (11) having optical black pixels and active clear pixels, wherein the pixel array (11) has lines of only optical black pixels, and lines containing both optical black pixels and active clear pixels, the circuit (100) comprising:

a differential programmable gain amplifier (210), one input of the differential programmable gain amplifier (210) connected to the pixel array output signal from the pixel array (11);

an analog-to-digital converter (220) connected to the differential programmable gain amplifier (210), wherein the analog-to-digital converter (220) converts (220) a programmable gain amplifier output signal from the programmable gain amplifier (210) into a digitized output signal;

a first summing block (310) connected to an output of the analog-to-digital converter (220);

a black clamp processing block (500) connected to the output of the analog-to-digital converter (220)~~summing block (310)~~, wherein the black clamp processing block (500) compares the digitized output signal with a black reference value, and outputs a black level adjustment signal to an input of the programmable gain amplifier (210);

a line noise correction processing block (400) connected to a second summing block (410), wherein the line noise correction processing block calculates (400) ~~a~~ line noise average values for black pixels in the digitized output signal on a line-by-line basis for lines containing both optical black pixels and active clear pixels, and lines containing only optical black pixels, and calculates ~~a~~ line noise offsets based on a difference between ~~the~~ each line noise average value and the black reference value; and

a column noise correction processing block (300), wherein the column noise correction processing block (300) calculates ~~a~~ column noise offsets ~~for black pixels~~ from the pixels of ~~all optical black~~ lines containing only optical black pixels in the digitized output signal, the column noise offsets calculated on a column-by-column basis by calculating a difference

between the digitized output signal for each black pixel of the column and the line noise average value of the line of the black pixel calculated by the line noise correction processing block (400),

wherein the first summing block (310) is configured to add the respective column noise offsets on a column-by-column basis to the clear pixels in the digitized output signal; and

the second summing block (410) is configured to add the line noise offsets on a line-by-line basis to the clear pixels in the digitized output signal."

"4. A method performed by the signal processing circuit (100) of claim 1 to process the output signal from the pixel array (11), the method comprising:

the black clamp processing block (500) calculating the black level adjustment signal by calculating a difference between the digitized output signal from the pixel array and the black reference value;

the line noise correction processing block (400) calculating the line noise correction values by calculating ~~a~~ line noise average values from black pixel values in the digitized output signal on a line-by-line basis for lines comprising both optical black and active clear pixels, and lines containing only optical black pixels;

the line noise correction processing block (400) calculating ~~a~~ line noise offsets based on a difference between the line noise average values and the black reference value;

the column noise correction processing block (300) calculating column noise offsets from the pixels of lines containing only optical black signals in the digitized output signal, the column noise offsets calculated on a column-by-column basis ~~the column noise correction value~~ by calculating a difference between

the digitized output signal for each black pixel of the column and the line noise average value of the line of the black pixel calculated by the line noise correction processing block (400);

the black clamp processing block (500) adjusting a black level in the output signal according to the black level adjustment signal to form a second output signal;

the first summing block (310) adding the respective column noise correction values on a column-by-column basis to the second output signal to form a third output signal;

the second summing block (410) adding the line noise ~~correction value~~offsets on a column by column basis to the third output signal, to form a fourth output signal; and

outputting the fourth output signal."

IX. Claim 1 according to the appellant's **second auxiliary request** reads as follows (additions to claim 1 of the **first auxiliary request** are underlined, deletions are ~~struck-through~~):

"A signal processing circuit (100) for processing an output signal from a pixel array (11), the pixel array (11) having optical black pixels and active clear pixels, wherein the pixel array (11) has lines of only optical black pixels, and lines containing both optical black pixels and active clear pixels, the circuit (100) comprising:

a differential programmable gain amplifier (210), one input of the differential programmable gain amplifier (210) connected to the pixel array output signal from the pixel array (11);

an analog-to-digital converter (220) connected to the differential programmable gain amplifier (210), wherein the analog-to-digital converter (220) converts

(220) a programmable gain amplifier output signal from the programmable gain amplifier (210) into a digitized output signal;

a first summing block (310) connected to an output of the analog-to-digital converter (220);

a black clamp processing block (500) connected to the output of the analog-to-digital converter (220), wherein the black clamp processing block (500) compares the digitized output signal with a black reference value, and outputs a black level adjustment signal to an input of the programmable gain amplifier (210), and wherein the first summing block and black clamp processing block are connected to the output of the analog-to-digital converter via a further summing block (710);

a line noise correction processing block (400) connected to a second summing block (410), wherein the line noise correction processing block calculates (400) line noise average values for black pixels in the digitized output signal on a line-by-line basis for lines containing both optical black pixels and active clear pixels, and lines containing only optical black pixels, and calculates line noise offsets based on a difference between each line noise average value and the black reference value; and

a column noise correction processing block (300), wherein the column noise correction processing block (300) calculates column noise offsets from the pixels of lines containing only optical black pixels in the digitized output signal, the column noise offsets calculated on a column-by-column basis by calculating a difference between the digitized output signal for each black pixel of the column and the line noise average value of the line of the black pixel calculated by the line noise correction processing block (400),

wherein the first summing block (310) is configured to add the respective column noise offsets on a column-by-column basis to the clear pixels in the digitized output signal; and

the second summing block (410) is configured to add the line noise offsets on a line-by-line basis to the clear pixels in the digitized output signal."

X. Claim 4 according to the appellant's **second auxiliary request** is identical to claim 4 of the **first auxiliary request**.

Reasons for the Decision

1. The appeal is admissible.

Main and first and second auxiliary requests - Article 84 EPC

2. In its communication under Article 15(1) RPBA, the board informed the appellant of its provisional opinion on the claims filed with the statement of grounds of appeal. It raised the following objections of lack of clarity under Article 84 EPC against claims 1 and 4 of each of the main, first and second auxiliary requests (see sections 12 to 14 of the communication):

"Main request - Article 84 EPC

12. Re claim 1

12.1 Claim 1 includes the following wording:

'a first summing block (310) connected to an output of the analog-to-digital converter (220);

a black clamp processing block (500) connected to the summing block (310)...'.

12.2 Under point 2.1.1. of the reasons for the decision the examining division apparently held that it was unclear from the above wording how the black clamp processing block (500) was connected to the summing block (310), all the more so in the light of the description and drawings because according to figure 9 it was connected to the input of the summing block whereas according to figure 6 it was connected to the output of the summing block.

12.3 The appellant argued that there was an obvious error in figure 6 and that it would have been clear to the skilled person that the black clamp processing block (500) was connected to the input of the summing block (310).

12.4 The board concurs with the examining division that it is not clear in claim 1 whether the black clamp processing block (500) is connected to the input or the output of the summing block (310). Moreover, it is also unclear in claim 1 whether the connection is an input or an output of the black clamp processing block. According to figures 6 and 9, it is an input of the black clamp processing block.

The board is not persuaded by the appellant's argument that the skilled person would have regarded the connection of the black clamp processing block (500) to the output, rather than to the input, of the summing block (310) in figure 6 as an obvious error. In the board's view, the skilled person might have found this connection in figure 6 odd, but would not necessary have considered it an error because it might have been an

unexplained design variation not significantly affecting the functioning of the signal processing circuit. In other words, the board does not regard the alleged error in figure 6 as an error which may be corrected under Rule 139 EPC.

12.5 In the board's view, claim 1 also lacks clarity for the following reasons:
(a) it is unclear in claim 1 what the inputs and outputs of the 'line noise correction processing block (400)' and the 'column noise correction processing block (300)' are connected to;
(b) the expression 'output signal' in the definition of the line noise correction processing block (400) in claim 1 does not make it clear whether it refers to the analog or digitized output signal;
(c) the wording of claim 1 does not make it clear that several line noise average values are calculated, i.e. one per line, and several column noise offsets are calculated, i.e. one per column.

13. Re claim 4

13.1 Claim 4 concerns 'A method performed by the signal processing circuit (100) of claim 1'.

13.2 The board understands the objections raised under points 2.1.2 to 2.1.4 of the reasons for the decision as meaning essentially that some of the method steps in claim 4 are inconsistent with some of the functions performed by the blocks of the signal processing circuit of claim 1.

13.3 The appellant essentially counter-argued that these apparent inconsistencies could be resolved by turning to the description.

13.4 The board concurs with the examining division that claim 4 is unclear for the following reasons:

Claim 1 concerns a signal processing circuit which is essentially defined by the circuit blocks it comprises, how these blocks are interconnected and the functions performed by these blocks.

Claim 4 concerns a 'method performed by the signal processing circuit (100) of claim 1' which is further defined by method steps and the indication of which block of the circuit of claim 1 performs which step.

The method of claim 4 is thus defined by the method steps explicitly stated in claim 4, but also by the method steps implicitly contained in the block functions stated in claim 1. Already for this reason, the board regards claim 4 as unclear because all the steps of the claimed method should be stated in the method claim rather than indirectly by reference to another independent claim of the device category. The present hybrid structure of claim 4 inherently makes it confusingly difficult to identify the steps of the claimed method, which the board regards as a non-compliance with the requirement of clarity of Article 84 EPC.

Moreover, the hybrid structure of the method of claim 4 also makes it unclear whether the claimed method is limited to being 'performed by the signal processing circuit (100) of claim 1' or whether it only has to be suitable to be performed by that circuit.

Finally, as noted by the examining division, several of the steps stated in claim 4 are different from the steps

stated in the block functions in claim 1. These inconsistencies in the wording of the steps cause a lack of clarity in claim 4. Since the claims should be clear by themselves, the appellant's argument that these inconsistencies may be resolved by studying the description and drawings, is not sufficient.

First and second auxiliary requests - Article 84 EPC

14. The objections under point 12.5(a) and in section 13 above also apply to the amended claims according to the first and second auxiliary requests."

3. The appellant did not reply in substance to the above objections, either by providing arguments or by way of amendments to the claims.

4. After deliberation on the case in the oral proceedings of 31 January 2019, the board affirms the above view, which it expressed in the communication under Article 15(1) RPBA, that claims 1 and 4 according to the main and first and second auxiliary requests do not meet the requirement of clarity of Article 84 EPC.

5. Accordingly, the appellant's main and first and second auxiliary requests are not allowable.

Request to remit the case to the department of first instance for further prosecution

6. Under Article 111(1) EPC, the board may either decide on the appeal or remit the case to the department which was responsible for the decision appealed.

7. In the present case, the examining division refused the application on the ground that claims 1 and 4 of the

then sole request did not meet the requirement of clarity of Article 84 EPC. The board has reviewed the reasons for the decision under appeal and has come to the conclusion that they are essentially correct and that these and/or related objections under Article 84 EPC apply to claims 1 and 4 of the main and first and second auxiliary requests before it on appeal. Hence, none of the main or first or second auxiliary request is allowable. Consequently, the further auxiliary request that the board remit the case to the department of first instance for further prosecution is without any object and therefore cannot be allowed either.

Conclusion

8. Since none of the appellant's requests is allowable, the appeal is to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

K. Boelicke C. Kunzelmann

Decision electronically authenticated