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Datasheet for the decision of 16 June 2020

Case Number: T 0698/14 - 3.4.03

Application Number: 10182703.8

Publication Number: 2264741

IPC: H01L21/04, H01L29/06, H01L29/417, H01L33/38

Language of the proceedings: EN

Title of invention:
Silicon carbide dimpled substrate

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56, 76(1), 84
EPC Art. 123(2)

Keyword:
Added subject matter beyond the content of parent application - after amendment - (no)
Claims - Support in the description - after amendment - (yes)
Inventive step - (yes)

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Decisions cited:
T 0696/14

Catchword:

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It can be changed at any time and without notic

Beschwerdekammern

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Case Number: T 0698/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 16 June 2020

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Elkington and Fife LLP Prospect House 8 Pembroke Road Sevenoaks, Kent TN13 1XR (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 27 November 2013 refusing European patent application No. 10182703.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Papastefanou
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing the European patent application No. 10 182 703.8 on the ground that neither the Main Request nor the Auxiliary Request before it fulfilled the requirements of Article 76(1) EPC 1973.

The application is a divisional application of the European patent application No. 07 709 682.4 (published as WO 2007/081964 A1 and dealt with in this board's decision T0696/14).

II. The appellant's (applicant's) final request was that the decision under appeal be set aside and that a patent be granted on the basis of the Main Request or of the Auxiliary Request.

III. The Main Request consists of the following application documents:

- claims 1 to 9 filed with letter of 15 May 2020
- description, pages 1 to 11 filed with letter of 15 May 2020
- figures, Sheets 1/6 t 6/6 as originally filed.

IV. Reference is made to the following documents, cited in the impugned decision:

D1: US 2002/0117681 A1
D5: US 2003/0062526 A1
D8: US 2005/0233539 A1
D9: US 2004/0051136 A1.

V. Claim 1 of the Main Request is worded as follows:

A semiconductor structure comprising:
a silicon carbide substrate (70) of a first conductivity type having a first main surface (12) and a second main surface (14) opposing the first main surface;
an active epitaxial layer (60) on the first main surface of the silicon carbide substrate;
an array of dimples (42) extending from the second main surface into the silicon carbide substrate toward the first main surface, wherein the array of dimples (42) extends entirely through the silicon carbide substrate (70);
an epitaxial silicon carbide layer (44) of a second conductivity type opposite the first conductivity type disposed within the dimples and on the second main surface; and
a metallization layer (24) overlying the second main surface of the silicon carbide substrate and within the dimples.

VI. The wording of the claims of the Auxiliary Request is not relevant for this decision.

VII. The appellant's main argument was that with the amendments carried out in appeal, the grounds for the refusal of the application had been overcome.

Reasons for the Decision

1. The invention

1.1 The invention relates to a semiconductor structure.

1.2 In high power semiconductor devices and LEDs, silicon carbide is a commonly used material for the substrate. With its relatively high thermal conductivity, silicon

carbide provides an effective heat sink. At the same time, however, silicon carbide has high electrical resistance, something that affects the performance of the semiconductor device.

1.3 In an effort to find a compromise between these two properties of silicon carbide, dimples are formed into the silicon carbide substrate (see for example Figure 1 of the application as published). In this way, a quantity of the silicon carbide is removed from the substrate, reducing its electrical resistance, while sufficient material is left so that the substrate continues to function effectively as a heat sink (see also paragraph [0003] of the application).

1.4 The claimed invention proposes a way to decrease further the resistance of the substrate without removing more material. This is achieved by adding an epitaxial silicon carbide layer on the back side of the substrate (see "44" in Figure 7 of the application). At the same time, the dimples are formed to extend entirely through the silicon carbide substrate. This added epitaxial silicon carbide layer has a conductivity which is opposite to the one of the silicon carbide substrate, in this manner achieving a reduction of the electrical resistance between the electrical contact and the active semiconductor layer(s).

2. *Main Request, added subject-matter and support by the description (Articles 76(1), 84 EPC 1973 and 123(2) EPC)*

2.1 Claim 1 of the Main Request finds basis in original claims 1, 2, 7, as well paragraph [0037] and Figure 7

of the application as originally filed.

2.1.1 The dependent claims are supported as follows:

Claim 2 finds basis in paragraph [0037] and Figure 7 of the application as originally filed.
Claim 3 finds basis in original claim 4.
Claim 4 finds basis in original claim 5.
Claim 5 finds basis in original claim 6.
Claim 6 finds basis in original claim 8.
Claim 7 finds basis in original claim 11.
Claim 8 finds basis in original claim 12.
Claim 9 finds basis in original claim 13.

2.1.2 The description has been adapted to the claims. Further amendments concern the deletion of a series of claim-like worded "clauses" from the last part of the description (see pages 12/20 to 17/20 as originally filed) and of the paragraph [0044] (as originally filed), which contained an unclear term ("spirit ...of the invention"). The page numbering has also been adapted accordingly.

2.1.3 The board is satisfied, therefore, that the application according to the Main Request meets the requirements of Article 123(2) EPC.

2.2 Regarding the objections under Article 76(1) EPC 1973 in the grounds for the refusal (see points 1.1 to 1.12 of the reasons of the impugned decision), the board notes that the examining division held that claim 1, which related to the embodiment of Figure 7 and paragraph [0037], should have included the features (see point 1.11 of the reasons of the impugned decision):

- *a silicon carbide substrate of a given conductivity type, providing an effective heat sink;*
- *dimples extending entirely through a substrate of a given conductivity to provide access to the active layer to provide a low resistance back contact;*
- *an additional silicon carbide substrate layer of conductivity type opposite to the conductivity type of the silicon carbide substrate in order to reverse the conductivity type of the substrate with respect to the active layer*.

2.2.1 The board is satisfied that claim 1 of the current Main Request comprises the omitted features identified by the examining division and considers that this objection has been overcome.

Hence, the application according to the Main Request fulfills the requirements of Article 76(1) EPC 1973.

2.3 The claims of the Main Request are directed to the embodiment described in paragraph [0037] and in Figure 7 of the application. Claim 1 defines that the dimples extend "*entirely through the silicon carbide substrate (70)*".

The combination of the epitaxial silicon carbide layer (44) on the second main (back) surface of the substrate (and within the dimples) with the dimples extending entirely through the substrate corresponds to the embodiment of Figure 7 and paragraph [0037].

The requirement that the claims be supported in the description (Article 84 EPC 1973) is, thus, fulfilled and the corresponding objection raised by the board in its communication of 30 September 2019 (see point 4)

has been overcome.

3. Since the Main Request on file complies with the requirements of Article 76(1) EPC 1973, it overcomes the sole ground for the refusal invoked in the decision under appeal.

Taking into account that the issue of inventive step was discussed during the first instance examination procedure (see for example annex to the summons to the oral proceedings and applicant's letter of 30 September 2013) and the need for procedural economy (appeal filed in 2014), the board decides to make use of the power conferred by Article 111(1) EPC 1973 and proceeds to decide the case on its merits, without remitting it to the examining division.

4. *Main Request, inventive step (Article 56 EPC 1973)*

4.1 Closest prior art

4.1.1 The examining division was of the opinion that the subject-matter of claim 1 then on file did not involve an inventive step in view of document D8 in combination with the skilled person's common general knowledge, as exemplified in document D9 (see point 4 of the annex to the summons to the oral proceedings before the examining division).

4.1.2 The board does not share this opinion of the examining division.

The objection of the examining division was based mainly on the embodiment shown in Figure 5 of D8.

The board notes that there is no indication of a dimple

("trench" in D8) into the substrate (41 in Figure 5). The examining division regarded the N-type drift layer 42 as the substrate, trenches 47 as the dimples and the N-type channel layer 48 as the doped epitaxial layer of the claims (see also paragraphs [0170] to [0173] of D8).

The board does not agree with the interpretation of D8 by the examining division. Such an interpretation might have been tenable with respect to the original claims of the application where there was only general mention of a "first layer" and an array of dimples extending into the first layer (see claim 1 as originally filed). In claim 1 of the current Main Request, however, there is a specific definition of an array of dimples extending into the silicon carbide substrate and this is clearly not the case in D8. Furthermore, the N-type channel (48 in Figure 5 of D8), which the examining division considered to correspond to the epitaxial silicon carbide layer (44) of the claims, has the same conductivity type as the substrate 41, in contrast to claim 1 of the Main Request.

The board is, thus, of the opinion that D8 is not suitable as a starting point for the skilled person because the semiconductor structure it describes differs significantly from the structure of the claims.

Document D9, mentioned also by the examining division in the same communication, describes a device similar to the one in D8 (see Figure 3 of D9). Thus D9 cannot be considered to be suitable as closest prior art, either.

4.1.3 The board considers that documents D1 and D5 are more appropriate as closest prior art because they describe

devices with more features in common with the claimed invention.

4.1.4 D1 discloses devices (see Figures 1 to 3; paragraphs [0025] to [0037] and [0050] to [0052]), which are similar to the one of the claims (compare with Figure 7 of the application). The layer on the second main (back) surface of the substrate and within the dimples (31 in Figure 3; see also paragraph [0052] of D1) is, however, a dielectric layer and not an epitaxial silicon carbide layer as in the claimed structure (layer (44) in Figure 7 of the application).

4.1.5 D5 also describes a semiconductor device similar to the one of the claims (see Figures 12 to 15). In this case, the layer (480) on the second main (back) surface of the substrate and within the dimples is a metallic seed layer (see paragraphs [0071]-[0072]).

4.2 Difference and technical problem

4.2.1 Following from points 4.1.4 and 4.1.5 above, the claimed semiconductor structure differs from the ones in D1 and D5 in the nature of the additional layer formed in the back side (second main surface) of the substrate and within the dimples.

4.2.2 In the claimed structure, the additional layer is an epitaxial silicon carbide layer with a conductivity opposite to the one of the silicon carbide substrate. This has the technical effect of decreasing the resistance of the substrate as a whole (i. e. between the electrical contact - metallization layer (24) - and the active epitaxial layer (60)), and thus improving the overall performance of the semiconductor structure while maintaining a high thermal conduction through the

substrate (see also appellant's letter of 1 October 2018, second page).

4.2.3 In D1 the additional layer (31 in Figure 3 of D1) on the second main (back) surface of the substrate (and within the dimples) is a dielectric layer aiming to isolate electrically portions of the back side contact (20b) in order to prevent shorting of the device (see paragraph [0052]).

4.2.4 In D5, the additional layer (480 in Figure 12) is a metallic layer, which serves as a seed layer for the electroplating or electro-less plating that follows in order to fill the cavity (416) with an additional thermally conductive material (see paragraph [0071]).

4.2.5 Starting from either D1 or D5, the skilled person is, thus, faced with the technical problem how to decrease the resistance of the substrate.

4.3 Solution and obviousness

4.3.1 This technical problem is not considered either in D1 or in D5.

Moreover, there is nothing in D1 nor in D5 that would prompt the skilled person to add an epitaxial silicon carbide layer on the second main (back) surface of the substrate in the corresponding semiconductor structure. Thus, he would not arrive at the claimed structure without exercising any inventive skills.

The teaching of D1 even goes in the opposite direction, since there is a dielectric layer (31) added between the electrical contact (20b) and the substrate (12).

4.3.2 Hence, the subject-matter of claim 1 of the Main Request involves an inventive step in the sense of Article 56 EPC 1973. Claims 2 to 9 depend directly or indirectly on claim 1 and therefore also inventive.

5. The board concludes, therefore, that the application and the invention to which it relates meet the requirements of the EPC and EPC 1973 and a European patent is to be granted according to Article 97(1) EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent in the following version:

    - Claims 1 to 9 filed with letter of 15 May 2020;
    - Description, pages 1 to 11 filed with letter of 15 May 2020;
    - Figures, Sheets 1/6 t 6/6 as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated