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Datasheet for the decision of 22 November 2018

Case Number: T 2291/14 - 3.4.03

Application Number: 06738542.7

Publication Number: 1883951

IPC: H01L21/04, H01L29/78, H01L29/24

Language of the proceedings: EN

Title of invention:
METHODS OF FABRICATING SILICON CARBIDE DEVICES HAVING SMOOTH CHANNELS

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56
EPC Art. 52(1), 123(2)

Keyword:
Amendments - added subject-matter (yes)
Inventive step - auxiliary request (yes)

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It can be changed at any time and without notice.

Decisions cited:

Catchword:

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Case Number: T 2291/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 22 November 2018

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Boult Wade Tennant LLP Verulam Gardens 70 Gray's Inn Road London WC1X 8BT (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 July 2014 refusing European patent application No. 06738542.7 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 06 738 542 on the grounds that the claimed subject-matter did not meet the requirements of Article 123(2) EPC. In the section entitled "Additional observations", the Examining Division also found *inter alia* that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC.

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request, filed with letter dated 22 October 2018, or on the 1st auxiliary request (claims 1-10 and an amended description) filed during oral proceedings, or on the 1st or 2nd auxiliary requests filed with letter dated 22 October 2018 (which now form the present 2nd and 3rd auxiliary requests).

III. The following documents are referred to:

D1: US 6 573 534 B1
D2: EP 1 306 890 A2
D5: JP 2000 082812 A
(a computer generated translation of D5, a copy of which was sent to the appellant, has been used to interpret this document)
D7: Modern Power Devices; B Jayant Baliga; John Wiley & Sons, 1987; title page, bibliographic page, pages 12-15.

IV. (i) Claim 1 of the main request reads as follows:

"A method of forming a silicon carbide power device, wherein the silicon carbide power device comprises a Metal Oxide Semiconductor Field Effect Transistor, the method comprising:
forming an n^- silicon carbide layer (12) on a silicon carbide substrate (10);
forming a p-type silicon carbide well region (14) on the n^- silicon carbide layer (12);
forming a buried region of p^+ silicon carbide (18) in the p-type silicon carbide well region (14);
forming an n^+ region (20) of silicon carbide on the buried region of p^+ silicon carbide (18), the n^+ region (20) providing a source region of the device, an initial channel region of the power device being adjacent the buried region of p^+ (18) and n^+ region (20) of silicon carbide;
forming, by implanting, an n-type region of silicon carbide (21) in the p-type silicon carbide well region (14) using a patterned mask (120), the initial channel region comprising the n-type region of silicon carbide (21) and a portion (31) of the p-type silicon carbide region (14) between the p^+ region of silicon carbide (18) and the n-type region (20);
forming an n^- region (19) on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region;
removing a portion of the n^- region (19) from on the n^- type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region so that a portion (19') of the n^- region (19) remains on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region to provide a reduction in a surface roughness of a final channel region;
forming an n^+ drain region on the substrate (10) opposite the n^- silicon carbide layer (12), wherein the

n^- silicon carbide layer (12) serves as a drift region of the silicon carbide power device, the n-type silicon carbide region (21) formed to extend through the p-type silicon carbide well region (14) to the drift region;
depositing a layer of insulating material (30) so as to provide a gate insulating material, the gate insulating material extending over the final channel region to the n^+ source region (20); and
forming a gate contact (26) by forming a metal contact on the gate insulating material (30),
wherein the final channel region includes the n-type region of silicon carbide (21), the portion (31) of the p-type silicon carbide well region (14) between the p^+ region of silicon carbide (18) and the n-type region (21) and the portion (19') of the n^- region (19) that remains on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region."

(ii) Claim 1 of the 1st auxiliary request filed at oral proceedings reads as follows:

"A method of forming a silicon carbide power device, wherein the silicon carbide power device comprises a Metal Oxide Semiconductor Field Effect Transistor, the method comprising:
forming an n^- silicon carbide layer (12) on an n^+ or n^- silicon carbide substrate (10);
forming a p-type silicon carbide well region (14) on the n^- silicon carbide layer (12);
forming a buried region of p^+ silicon carbide (18) in the p-type silicon carbide well region (14);
forming an n^+ region (20) of silicon carbide on the buried region of p^+ silicon carbide (18), the n^+ region (20) providing a source region of the device, an initial channel region of the power device being

adjacent the buried region of p^+ (18) and n^+ region (20) of silicon carbide;
forming, by implanting, an n-type region of silicon carbide (21) in the p-type silicon carbide well region (14) using a patterned mask (120), the initial channel region comprising the n-type region of silicon carbide (21) and a portion (31) of the p-type silicon carbide region (14) between the p^+ region of silicon carbide (18) and the n-type region (21);
forming an n^- region (19) on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region;
removing a portion of the n^- region (19) from on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region so that a portion (19') of the n^- region (19) remains on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region to provide a reduction in a surface roughness of a final channel region; and
removing a portion of the remaining n^- region (19') such that the remaining n^- region (19') is removed from the n^+ region (20);
wherein the final channel region includes the n-type region of silicon carbide (21), the portion (31) of the p-type silicon carbide well region (14) between the p^+ region of silicon carbide (18) and the n-type region (21) and the portion (19') of the n^- region (19) that remains on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region."

Reasons for the Decision

1. The appeal is admissible.

2. *Main request: Article 123(2) EPC*

2.1 Claim 1 comprises the feature "forming an n^- silicon carbide layer (12) on a silicon carbide substrate (10)". Although this feature was present in claim 1 as originally filed, present claim 1 is based not merely on the original claims, but on the method depicted in Figs. 2A-2J and explained in the accompanying text of the description.

In the description and drawings, only two specific conductivity types for the silicon carbide substrate are disclosed: n^- (see paragraphs [0016], [0033] and claims 16, 17 of the application as filed), and n^+ (see paragraph [0032] of the application as filed and the figures). Numerous features have been imported into claim 1 from the embodiments of the description and drawings, without importing the substrate conductivity types with which they are disclosed. Indeed, according to claim 1, the silicon carbide substrate need not even be n-type. In the opinion of the Board, this results in an inadmissible intermediate generalisation.

2.2 Moreover, according to claim 1, the method involves "forming an n^+ drain region on the substrate". The formation of such a region is only disclosed in the application as filed in the case that the substrate is of conductivity type n^- (see paragraphs [0016], [0033] and claims 16, 17). Claim 1 includes embodiments comprising the formation of an n^+ drain region in combination with substrates of conductivity type other than n^- . No such embodiments are disclosed in the application as filed.

2.3 Claim 1 discloses the feature:

"depositing a layer of insulating material (30) so as to provide a gate insulating material, the gate insulating material extending over the final channel region to the n^+ source region (20)".

The Board sees no support for defining the formation of the gate insulating layer at this level of generality. The only disclosure of the formation of a gate insulating layer is in paragraphs [0056] and [0057], which define *inter alia* depositing an insulating layer over the whole device, forming contact holes therein and forming ohmic contacts in the contact holes to provide source contacts. Claim 1 therefore defines the formation of the gate insulating layer at a level of generality which is not present in the application as filed.

2.4 For the reasons given above, claim 1 of the main request fails to meet the requirements of Article 123(2) EPC.

3. *1st auxiliary request: Article 123(2) EPC*

3.1 Claim 1 of the 1st auxiliary request is based on claims 1 and 18 as originally filed, Figs. 2A-2J and the following paragraphs of the original description: [0035], [0036], [0047], [0052] and [0054]. The problems identified in relation to claim 1 of the main request have been overcome by amendment.

3.2 Dependent claims 2-10 are based on claims 2, 3, 6-9 and 11-13 as originally filed; the description has been suitably adapted. The 1st auxiliary request is therefore considered to meet the requirements of Article 123(2) EPC.

4. *1st auxiliary request: Inventive step*

4.1 In the contested decision the closest prior art was seen as D5, in particular the fourth embodiment (i.e. the manufacturing steps depicted in Figs. 8-10, which lead to the device of Fig. 7). The Board sees no reason to question this choice.

4.2 Before commencing a formal problem-solution analysis, the Board wishes to turn briefly to the question of how the terminology used in claim 1 is to be understood, both in relation to the claimed invention and in the context of the prior art.

Claim 1 is directed to a method of forming a silicon carbide power device comprising a MOSFET (Metal Oxide Semiconductor Field Effect Transistor). As is well-known, such devices comprise an element known as the "channel" which lies under the gate insulating layer, whereby the conductivity of the channel (or at least that part of it nearest the gate insulator) may be modulated by applying a voltage to the gate electrode, thereby opening or closing a conductive path between the source and drain regions.

The skilled person would recognise that, with the exception of the features of forming and partially removing the n^- region 19, claim 1 defines standard steps in the manufacture of a "double diffused MOSFET" (DMOSFET), as mentioned in paragraph [0005] of the description and depicted in Fig. 1. For such a device, the skilled person would understand that the p^- type region 31 (or at least the upper part of it) forms the channel, i.e. an inversion region which, under the

influence of a suitable applied gate voltage, completes a conductive path between source and drain.

4.3 In claim 1 and throughout the description the term "channel region" is used to refer to regions which comprise the channel, together with layers which are in close proximity to the channel, but which themselves do not constitute part of the physical channel (i.e. they do not function to open or close a conductive path between source and drain under the influence of an applied gate voltage).

For example, in parts of the application as filed (e.g. claim 1 and paragraph [0050], first sentence; paragraph [0051], final sentence and paragraph [0054], first sentence in combination with Fig. 1) the n^- region (19/19') is said to be formed "on" (hence, not forming part of) the channel region. The channel region thus defined appears to comprise the combination of the n-type silicon carbide region 21 and the p-type region 31 (the actual physical channel). In claim 1 this combination has been labelled "the initial channel region".

Elsewhere (see e.g. paragraph [0038], first sentence; paragraph [0039], second sentence and paragraph [0051], first sentence) a channel region is defined as comprising the n-type silicon carbide region 21 and the p-type region 31 *in combination with* the remaining portion of the n^- region 19'. In claim 1 this combination has been labelled "the final channel region".

The Board has no objection to the terms "channel region", "initial channel region" and "final channel region", these terms being understood in the above

sense. However, it must be stressed that, according to this terminology, for a region to qualify as a "channel region" it must at least include the actual physical channel.

4.4 Document D5 also discloses a silicon carbide vertical power MOSFET, although the operating principle is rather different.

In this arrangement the n^- layer 5 forms the channel ("surface channel layer"). As explained in relation to the embodiment of Fig. 1 (see paragraphs [0077]-[0080] and [0088]-[0091]), the thickness of the surface channel layer 5 is such that, in the OFF state, the ends of the surface channel layer adjacent the p-type base region 3 are entirely depleted due to the built-in voltage of the PN junction formed by the surface channel layer 5 and the p-type base region 3 (also taking into account the work function of the gate electrode 8). Current from the source to the drain region is therefore blocked.

When a positive bias is applied to the gate electrode 8, the device switches to its ON state and current flows from the n^+ type source region 4 via the surface channel layer 5 to the n^+ type drain region 1 (see paragraph [0090]).

4.5 Hence, the channel in D5 consists of the "surface channel layer" 5 *only*. In particular, in the arrangement of Figs. 7-10, neither the p^- type base region 3a nor the part 2a of the epi (drift) layer (lying between regions 3a in Fig. 7) functions as a channel.

4.6 In the "Additional observations", the Examining Division argued that D5 disclosed all features of claim 1 except "removing a portion of the n^- region (19) ... to provide a reduction in a surface roughness of the channel region". The problem was to improve carrier mobility, and since it was known that this could be achieved by reducing the roughness of the channel region, "the skilled person starting from D5 would thus be motivated to remove a portion of the n-region (5) of D5 from the channel region to reduce its surface roughness", thus rendering the distinguishing feature obvious.

4.7 The Board is also of the view that it is common knowledge in the art that reducing the surface roughness of the interface between the channel and the gate insulator increases carrier mobility and thereby improves device performance, as described, for example, in D7 (an excerpt from a well-known textbook in the field).

4.8 In D5, the surface on which channel layer 5 is deposited is first "planarized", and the channel layer is deposited by epitaxy (paragraphs [0125] and [0130]), and hence the upper surface of the channel layer would already be relatively smooth. Nevertheless, it is unlikely that the level of smoothness envisaged in the present application (see e.g. claim 6 as originally filed) would be achieved without further measures, and hence it is not implausible that the skilled person would consider an additional step of reducing the surface roughness of the surface channel layer.

Commonly known methods of reducing surface roughness typically involve mechanical means (grinding, polishing), chemical means (etching) or chemical

mechanical means (CMP, as mentioned in the description), all of which involve the removal of a portion of the layer (i.e. the peaks or protuberances).

4.9 The Board therefore agrees that it would be obvious for the skilled person to act in the manner suggested by the Examining Division. The question, however, is whether this would result in the skilled person carrying out a method corresponding to that defined in claim 1.

4.10 Claim 1 defines "forming an n^- region (19) on the n-type region of silicon carbide (21) and the p-type silicon carbide region (31) of the initial channel region" and subsequently "removing a portion of the n^- region (19)". In D5 the n^- surface channel layer 5 is formed on the p^- type base region 3a and the part 2a of the epi (drift) layer. As mentioned above, neither of these regions corresponds to the channel, and D5 does not therefore disclose the formation of an n^- region on a channel region, as claimed.

4.11 Consequently, starting from D5, reducing the thickness of the layer 5 after deposition would be an obvious measure for the skilled person. However, this would correspond to reducing the thickness of the channel itself - a different solution to the problem from that currently claimed. According to the claimed invention, the reduction in surface roughness is carried out via what the appellant refers to as a "two-step process": forming an n^- region on an initial channel region (i.e. on a region comprising the channel) and subsequently removing a portion of the n^- region. This measure is not disclosed or suggested in D5.

4.12 Document D2 discloses *inter alia* methods for manufacturing MOSFETs.

4.13 A first method is described in paragraphs [0277]-[0298] and depicted in Figs. 14A-14C. An n-type doped layer 192 is grown on a substrate (Fig. 14A; paragraph [0280]), and is then subjected to annealing in a hydrogen atmosphere to flatten the macro steps 191 formed on the top face of the n-type doped layer (Fig. 14B; paragraph [0282]). Subsequently, a channel layer is formed during formation of a p-type well 195 in the n-type doped layer 192 by ion implantation (Fig. 14C; paragraph [0283]); the skilled person would understand that the channel would correspond to that part of the p-type well proximate to the gate insulating film 199.

Although the flattening of the macro steps 191 of the n-type doped layer 192 would involve removing a portion of this layer, this annealing step takes place prior to the formation of the channel (hence, prior to the existence of any channel region). It does not, therefore, correspond to a removal of a portion of an n^- region formed on an initial channel region, as claimed in the present first auxiliary request.

4.14 In other embodiments of D2 (e.g. Figs. 5A-5C, 15A-15C), MOSFETs are disclosed comprising multilayer structures (71, 205) of alternating δ-doped SiC layers and low concentration doped SiC layers. Methods are disclosed for "suppressing the formation of macro steps" in the multilayer parts (paragraph [0175], first sentence; paragraph [0310]).

However, in all such embodiments, the multilayer structures define the channel (paragraphs [0104], [0181], [0311] and [0320]). The layers on which the

multilayer structures are deposited (the p-type well 65 and n-type doped layer 62 in Figs. 5A-5C, and the p-type doped layer 202 in Figs. 15A-15C) do not constitute or comprise the channel.

Hence, these embodiments of D2 may be considered to disclose flattening procedures involving the removal of material from various layers including the (multilayer) channel, but they do not disclose forming an n^- region *on a channel region* and removing a portion of it.

4.15 The Board can accept the appellant's argument that the claimed two-step process may offer advantages over simply smoothing the (initial) channel region. The deposited n^- region is provided solely to be reduced in thickness to thereby improve the surface smoothness of the channel region. Accordingly, it can be deposited by any convenient method to a thickness which may be optimised to allow removal of a desired amount of material to achieve a target value for the surface roughness. The channel *per se* can be formed without being subject to any constraints imposed by surface roughness requirements.

4.16 The Board therefore judges that the subject-matter of claim 1 of the 1st auxiliary request involves an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   Claims 1-10 of the "New 1st Auxiliary Request" filed during oral proceedings;

   Description: pages 1 - 17 filed during oral proceedings;

   Figures: sheets 1 - 8 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated