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Datasheet for the decision of 8 April 2020

Case Number: T 1540/15 - 3.4.03

Application Number: 02745704.3

Publication Number: 1407490

IPC: H01L25/065, H01L23/538

Language of the proceedings: EN

Title of invention:
SINGLE PACKAGE CONTAINING MULTIPLE INTEGRATED CIRCUIT DEVICES

Applicant:
Taiwan Semiconductor Manufacturing Co., Ltd.

Headword:

Relevant legal provisions:
EPC Art. 123(2)
EPC 1973 Art. 84, 56

Keyword:
Amendments - added subject-matter (no)
Clarity (no)
Inventive step - (no)

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Case Number: T 1540/15 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 8 April 2020

Appellant: (Applicant)	Taiwan Semiconductor Manufacturing Co., Ltd. No. 8, Li-Hsin Rd. 6 Science-Based Industrial Park Hsin-Chu, 300-77 (TW)
Representative:	Nederlandsch Octrooibureau P.O. Box 29720 2502 LS The Hague (NL)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 16 March 2015 refusing European patent application No. 02745704.3 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Ley
	T. Bokor

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division to refuse European patent application No. 02 745 704.3.

The examining division decided that the sole main request (independent claims 1 and 5 filed with the letter of 3 February 2015) lacked an inventive step (Article 56 EPC 1973).

II. The appellant requested to set aside the decision and to grant a European patent on the basis of either a main request filed with a letter dated 3 February 2015 or an auxiliary request filed with the statement of the grounds of appeal. The appellant requested oral proceedings in case "the Board of Appeal contemplates a decision that does not fully meet the Appellant's requests".

III. The Board issued a summons to oral proceedings scheduled to take place on 12 March 2020.

In a communication pursuant to Article 15(1) RPBA 2007 dated 11 November 2019 the Board gave its provisional opinion that claims 1 and 5 according to the main request did no comply with Articles 123(2) EPC and 84 EPC 1973 and that the subject-matter of claims 1 and 5 according to the main request and the auxiliary request did not involve an inventive step (Article 56 EPC 1973).

IV. In a letter dated 5 February 2020, the appellant withdrew its request for oral proceedings and informed Board that neither the appellant nor its representative

would attend oral proceedings and that it wished "to receive a decision according to the present state of the file". No further submissions were made.

V. The Board cancelled the oral proceedings.

VI. Device claim 1 according to the main request reads as follows (labelling **(a)** to **(j)** added by the Board):

An integrated circuit device package (10)comprising
(a) *a substrate (100),*
(b) *a first device (2) and*
(c) *a second device (4),*
(d) *which devices (2, 4) are present on the substrate (100) are provided in an encapsulation (6),*
(e) *a first set (22) of external electrical connection contacts and a second set (24) of external electrical connection contacts are in the form of an array of solder balls (16),*
(f) *in which the first set (22) and second set (24) of external electrical connection contacts are separated by spacing gaps (26, 28) there between,*
(g) *wherein the substrate (100) comprising a signal layer (34), a ground layer (38), a power layer (44) and the bottom layer (48),*
(h) *each of which comprises a first set of electrical connection nodes and traces (52, 62, 72, 82) and a second set of electrical connection nodes and traces (54, 64, 74, 84), and*
(i) *the first set of electrical connection nodes and traces (52, 62, 72, 82) and the second set of electrical connection nodes and traces (54, 64, 74, 84) are separated by further spacing gaps (58, 68, 78, 88),*
(j) *wherein first and second devices (2, 4) are connected to the first set (22) of external electrical connection contacts and the second set (24) of external*

electrical connection contacts, respectively, through the first set of electrical connection nodes and traces (52, 62, 72, 82) and the second set of electrical connection nodes and traces (54, 64, 74, 84) of the signal layer (34), a ground layer (38), a power layer (44) and the bottom layer (48).

Method claim 5 according to the main request reads as follows (labelling **(i)** to **(viii)** added by the Board):

A method of packaging semiconductor devices (2, 4) comprising:
***(i)** placing a first device and a second device (2, 4) respectively on a first section and a second section (52, 54) of a top layer of a substrate (100) of a single ball grid array package (10),*
***(ii)** each first and second device (2, 4) having a plurality of electrical terminals,*
***(iii)** each first and second section (52, 54) having a plurality of electrical connections for connecting the terminals of the respective first and second devices to external electrical connection contacts (22, 24) of a bottom layer of a substrate of the package (10),*
***(iv)** creating spacing gaps (26, 28) between the external electrical connection contacts (22, 24) by removal of predetermined external electrical connection contacts to maintain electrical isolation among the plurality of electrical connections; and*
***(v)** providing an encapsulation (6) to encapsulate the first and second devices (2, 4), wherein*
***(vi)** the substrate (100) comprising a signal layer (34), a ground layer (38), a power layer (44) and the bottom layer (48),*
***(vii)** each of which comprises a first set of electrical connection nodes and traces (52, 62, 72, 82) and a*

second set of electrical connection nodes and traces (54, 64, 74, 84), and
(viii) *the first set of electrical connection nodes and traces (52, 62, 72, 82) and the second set of electrical connection nodes and traces (54, 64, 74, 84) are separated by further spacing gaps (58, 68, 78, 88).*

VII. Claims 1 and 5 of the auxiliary request differ from claims 1 and 5 of the main request only by specifying that the first set of electrical connections nodes and traces and the second set of electrical connections nodes and traces are electrically isolated.

Reasons for the Decision

1. The appeal is admissible.

2. Procedural issues

In preparation for the oral proceedings the Board issued its preliminary opinion on the case raising objections against all requests under Articles 123(2) EPC, 84 EPC 1973 and 52(1) EPC in combination with Article 56 EPC 1973.

As the appellant chose not to comment on the preliminary opinion issued by the Board in preparation of the oral proceedings and as it withdrew its request for oral proceedings, the Board does not see any reason to deviate from its preliminary opinion and concludes that the case is ready for decision.

3. Added subject matter - Article 123(2) EPC

3.1 Features (g) to (i) in claim 1 of both requests are disclosed in the application as originally filed only

in the embodiment shown in figures 3 and 4A - 4D. The embodiment of figures 3 and 4A to 4D is limited to the arrangement first, second IC devices 2, 4 - signal layer 34 - ground layer 38 - power layer 44 - bottom layer 48 - solder balls 16. From the layouts shown in figures 4A - 4D, the skilled person would understand that, for example, the order of the ground layer 38 and the power layer 44 cannot be reversed. The Board could not find any indication in the application as filed that the order of layers 34, 38, 44, 48 could be different from the one shown in figure 3.

As the order of the different layers (i.e. signal, ground, power and bottom layers) is not specified in claim 1, the Board finds that claim 1 of both the main request and the auxiliary request is directed at an unallowable intermediate generalisation of the embodiment shown in figures 3, 4A to 4D so that the requirements of Article 123(2) EPC are not met.

3.2 For the reason given in previous section 3.1, *mutatis mutandis*, the requirements of Article 123(2) EPC are not met for method claim 5 of both the main request and the auxiliary request.

In addition, in method claim 5, it is not even specified that the first and second devices 2, 4 are connected to the first set of external electrical connection contacts 22 and the second set of external electrical connection contacts 24, respectively, through the first set of electrical connection nodes and traces 52, 62, 72, 82 and the second set of electrical connection nodes and traces 54, 64, 74, 84 of the signal layer 34, a ground layer 38, a power layer 38 and the bottom layer 48.

In other words, the wording of claim 5 leaves it open how the connection between the devices 2, 4 and the external electric connection contacts (= solder balls 16 in sections 22, 24) is achieved. Also for this reason, the requirements of Article 123(2) EPC are not fulfilled.

4. In its communication under Article 15(1) RPBA 2007, the Board also gave its provisional opinion that the requests on file did not appear to meet the requirements of clarity (Article 84 EPC 1973) and inventive step (Article 52(1) EPC and Article 56 EPC 1973).

As the Board has no reason to deviate from its provisional opinion, the requests on file are also not allowable for these reasons.

5. Since none of the requests on file is allowable, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated