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Datasheet for the decision of 18 October 2021

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Language of the proceedings:	EN

Title of invention:
Device for controlling electrical conduction across a semiconductor body

Applicant:
Cree, Inc.

Relevant legal provisions:
EPC Art. 52(1), 54(1), 54(2)
RPBA 2020 Art. 13(2), 25(1)

Keyword:
Novelty - main request (no)
Amendment after summons - auxiliary request - taken into account (no)

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Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 1790/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 18 October 2021

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	FRKelly 27 Clyde Road Dublin D04 F838 (IE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 15 March 2016 refusing European patent application No. 12162732.7 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Ley
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. EP 12 162 732 pursuant to Article 97(2) EPC. It is a European divisional application in the sense of Article 76 EPC of earlier European patent application EP 09 151 203 (hereinafter: the parent application).

The following document was *inter alia* cited:

D1 JP 2001 094097 A

The examining division decided that claims 1 and 10 according to the main request did not fulfil the requirements of Article 76(1) EPC, that the subject-matter of claim 1 was not new (Article 52(1), 54(1) and (2) EPC) and that the subject-matter of claim 10 did not involve an inventive step (Article 52(1) EPC, Article 56 EPC).

For claims 1 and 10 according to a first auxiliary request, the examining division arrived at the same conclusion. Regarding a second auxiliary request, the examining division held that claims 1 and 9 did not meet the requirements of Article 76(1) EPC and were not allowable in view of a lack of inventive step (Article 52(1) EPC, Article 56 EPC) for claims 1 and 9.

II. In a communication pursuant to Article 15(1) RPBA dated 6 April 2020, the Board informed the appellant that the main request filed with the statement setting out the grounds of appeal did not meet the requirements of the EPC.

III. With a letter dated 23 October 2020, the appellant filed a modified main request and an auxiliary request.

IV. The appellant requests that the impugned decision be set aside and a European patent be granted on the basis of the main request or auxiliary request, both filed with said letter dated 23 October 2020. In the alternative, the appellant requests that the application be remitted to the examining division for further examination.

V. With a short letter dated 28 September 2021, the appellant informed the Board that it would not attend the oral proceedings scheduled for 22 October 2021.

The Board then cancelled the oral proceedings.

VI. Claim 1 according to the main request has the following wording (Board's labelling):

A device for controlling electrical conduction across a semiconductor body, comprising:
(a) *a source or emitter region (38, 78) having a first conductivity type within the semiconductor body;*
(b) *a well region (33, 34) having a second conductivity type and positioned adjacent said source region;*
(c) *a JFET region (61, 87) adjacent a side of said well region opposite said source region, said JFET region having said first conductivity type for providing a conductive path for carriers from said source region; characterized in that the device further comprises:*
(d) *an epitaxial channel layer (46, 66) having the first conductivity type and the second conductivity type,*

(d1) *the epitaxial channel layer on at least a portion of said source, well, and JFET regions, to provide a conductive path across said well region to said JFET region,*

(d2) *wherein the epitaxial channel layer is the first conductivity type on the source and JFET regions and the epitaxial channel layer is the second conductivity type on the well region,*

the epitaxial channel layer comprises:

(d3) *a first channel layer region (56, 70) on said source region (38), wherein the first channel layer region is doped at a first doping level within the epitaxial channel layer such that the first channel layer region has the first conductivity type;*

(d4) *a second channel layer region (57, 71) having the first conductivity type on said source region (38), the second channel layer region (57, 71) being doped at a second doping level that is less than the first doping level of the first channel layer region (56, 70), where the first and second channel layer regions are configured to provide carriers across the epitaxial channel layer; and*

(d5) *a threshold voltage regulating region (58, 72) that is epitaxially grown with the second conductivity type, said threshold voltage regulating region (58, 72) being adjacent said second channel layer region (57, 71) and on said well region;*

(d6) *a third channel layer region (60, 73) of the first conductivity type adjacent the threshold voltage regulating region (58, 72) opposite the second channel layer region (57, 71) where the third channel layer region (60, 73) is disposed on the JFET region; and*

(e) *a control contact (45, 85) on said channel layer for controlling current from said source region across said JFET region.*

Claim 1 according to the auxiliary request corresponds to claim 1 according to the main request, wherein the following feature is added its end:

(g) and *wherein an inversion channel region is formed in both the threshold voltage regulating region (58, 72) and a top region (31) of the well section (33) when a voltage is applied to the control contact (45, 85).*

VII. The appellant's arguments can be summarized as follows:

(a) Main request

In the statement setting out the grounds of appeal, the appellant argued that the independent claims differed from D1 by a third channel layer region that extended only on a JFET conduction region (i.e. the upper portion (61) of the drift region 54). Since the channel layer (46) was divided into sections, or regions, it allowed a better control over a threshold voltage that regulated current from source to drain, or similarly from the emitter to the collector. In the channel layer (46), the n+ source (38) provided carriers for conduction from the source (38), through the N-type first channel layer region (56) to the channel zone (50) of the P-type threshold voltage regulating region (58). The carriers then moved across the drift region (54) toward the collector (42). The first channel layer region (56) along with threshold voltage regulating region (58) added additional levels of control that allowed the voltage on the gate or control contact (45) to accurately manipulate the magnitude of the current conducting through the device (30). The first channel layer region (56) extended on at least a portion of the source (38)

while the threshold voltage regulating region (58) extended on the well region (33) to provide additional carriers across the conductive channel (50). As the threshold voltage regulating region (58) was completely on the well region (33), a threshold voltage inverted the threshold voltage regulating region (58) to create the conductive channel (50). By having a third channel layer region (60) only on a JFET region, this allowed the threshold voltage regulating region (58) to provide a better control of the threshold voltage that regulated current. Therefore, the objective technical problem to be solved was how to control conduction in a semiconductor device.

In its letter dated 23 October 2021, the appellant argued that D1 did not disclose a threshold voltage regulating region that was epitaxially grown with said second conductivity type on said at least one well region, said second conductivity type being opposite to the first conductivity of the drift region. In D1, channel layer 5a, 5b was grown with the same conductivity type as the drift region and then submitted to a step of ion implantation to form region 5b, see figures 5(a) and 5(b) of D1. Such configuration might suffer from fluctuations in the threshold voltage that turned ON the device, at least partly due to temperatures variations. The technical effect would be to provide a higher threshold voltage than the prior art devices of D1. The higher threshold voltage provided greater assurance that the device would be normally OFF at a gate bias of zero volts for all operating temperatures.

(b) Auxiliary request

D1 did not disclose feature (g). The technical effect would be a thicker inversion channel region and thus a reduction in device channel resistance, see paragraph [0037] of the application. Paragraphs [0078] to [0081] of D1 described that the depletion region was formed at the interface between channel layer 5b and gate oxide 7. It did not extend into the underlying p-type region 41.

Reasons for the Decision

1. The appeal is admissible.

2. The appellant's declared intention not to attend the oral proceedings is considered by the Board as equivalent to a withdrawal of its request for oral proceedings (see Case Law of the Boards of Appeal of the European Patent Office, 9th Edition, 2019, III.C. 4.3.2).

Taking into account the appellant's arguments provided in its letter dated 23 October 2020, the Board concludes that the case is ready for decision without oral proceedings.

3. The invention concerns a device for controlling electrical conduction across a semiconductor body, like e.g. a power transistor. The device has an epitaxial channel layer (46/66, 56/70, 57/71, 58/72, 60/73) divided into sections of varying conductivity type and doping level (see figures 2 and 3). The epitaxial channel layer provides a conductive path from a source

(38/78) or emitter region (78) across a well region (33/83, 34/84) to a drift region or JFET region (61/87), see figures 2 and 3.

4. Main request

4.1 Added subject-matter - Article 76(1) EPC

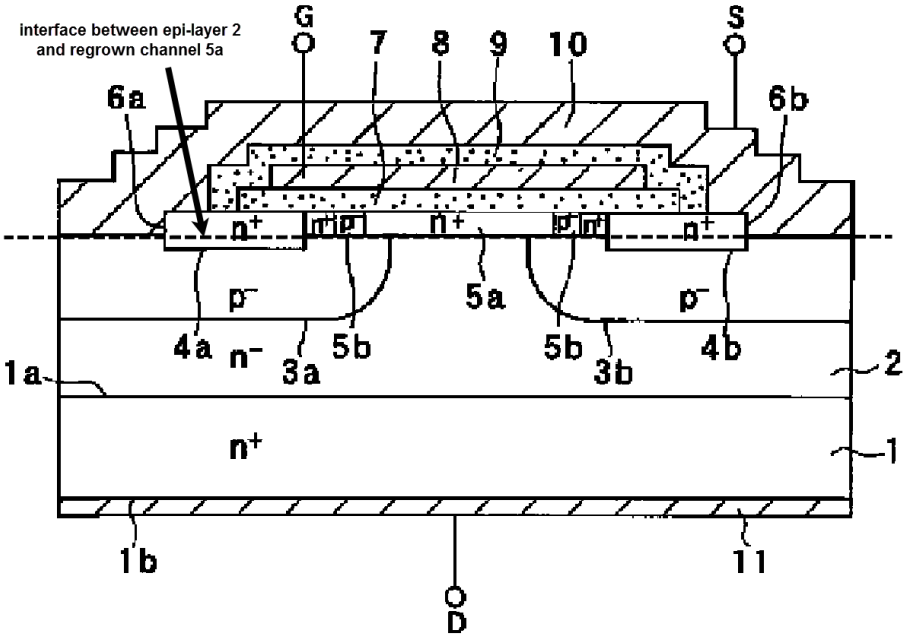
In the impugned decision, the examining division objected that the device of claim 1 according to the main request and its manufacturing method according to claim 10 did not specify that the doping level of the second channel layer region was less than the doping level of the first channel layer region, see point 1.2 of the decision. The examining division further stated that the wording of claims 1 and 10 suggested that channel parts having the second conductivity type could cover any part within the semiconductor body, contrary to what is shown in figures 2 and 3, see point 1.1 of the decision.

The Board is of the opinion that the amendments made to claim 1 according to its present wording overcome the examining division's objections under Article 76(1) EPC.

The Board is also satisfied that the amendments made to claim 1 overcome the Board's objections under Article 76(1) EPC raised in section 4.3.1 and the objection under Article 84 EPC raised in section 5.1 and 5.2 of the communication according to Article 15(1) RPBA 2020. The Board understands that the JFET region 61 is the upper portion of the drift region 61, 54, see paragraph [0039] of the application as filed (paragraph [0054] of the application as published).

4.2 Novelty - Articles 52(1), 54(1) and (2) EPC

4.2.1 In D1, the basic structure of the device of figure 9 is a silicon carbide substrate 1 with an epi-layer 2,onto which an epitaxial channel 5a is grown, see figure 4(c) or see the annotated figure 9 provided by the Board with an indication of the position of the interface the epi-layer 2 and the epitaxially-regrown channel 5a.



The Board therefore agrees with the examining division that region 4a can be divided into two parts: an upper part within epitaxial channel 5a, which corresponds to the first and second channel layer regions, and a lower part within epi-layer 2, which corresponds to the source region.

The Board further agrees with the examining division that the device of figure 9 must have an "intermediate" n-type region with lower impurity concentration (as compared e.g. to the center of region 4a) at the border

between the first channel layer (upper part of 4a) and the threshold regulating region (5b). Hence, a second channel layer region in the sense of claim 1 with lower doping level as compared to the first channel layer region is disclosed in D1.

Hence, D1 discloses (figures 1, 4 to 7, 9) a device for controlling electrical conduction across a semiconductor body, comprising:
a source or emitter region (lower part of 4a within epi-layer 2) having a first conductivity type (n, [0047], [0067]) within the semiconductor body (2, figure 4(a));
a well region (3a within epi-layer 2) having a second conductivity type (p, [0046], [0064]) and positioned adjacent said source region (figure 9);
a JFET region (part of 2 between 3a, 3b, figure 9) adjacent a side of said well region (3a) opposite said source region (lower part of 4a within epi-layer 2), said JFET region (part of 2 between 3a and 3b) having said first conductivity type (n) for providing a conductive path for carriers from said source region (lower part of 4a within epi-layer 2);
wherein the device further comprises:
an epitaxial channel layer (5a, figure 4(c)) having the first conductivity type (figure 9) and the second conductivity type (figure 9),
the epitaxial channel layer on at least a portion of said source, well, and JFET regions, to provide a conductive path across said well region to said JFET region (figure 9),
wherein the epitaxial channel layer is [of] the first conductivity type (n) on the source and JFET regions and the epitaxial channel layer is [of] the second conductivity type on the well region (figure 9),
the epitaxial channel layer comprises:

a first channel layer region (upper part of 4a within channel layer 5a) on said source region (lower part of 4a), wherein the first channel layer region is doped at a first doping level within the epitaxial channel layer such that the first channel layer region has the first conductivity type (figure 9);
a second channel layer region (upper part of 4a at the interface between 4a and 5b) having the first conductivity type on said source region (lower part of 4a within epi-layer 2), the second channel layer region being doped at a second doping level that is less than the first doping level of the first channel layer region (implicit), where the first and second channel layer regions are configured to provide carriers across the epitaxial channel layer (figure 9); and
a threshold voltage regulating region (5b) that is epitaxially grown "with" the second conductivity type (p), said threshold voltage regulating region (5b) being adjacent said second channel layer region (figure 9) and on said well region (3a);
a third channel layer region (5a) of the first conductivity type adjacent the threshold voltage regulating region (5b) opposite the second channel layer region (figure 9) where the third channel layer region (5a) is disposed on the JFET region (part of 2 between 5a and 5b); and
a control contact (8, G) on said channel layer (figure 9) for controlling current from said source region across said JFET region (figure 9).

4.2.2 Claim 1 according to the main request has been amended after the Board's objections under Article 76(1) EPC, see the communication, section 4.3.1. The feature that the third channel region extends only on a JFET region (see VII.(a), first paragraph), said JFET region being

the upper portion of the drift region, is not longer in claim 1.

Regarding the other alleged distinguishing feature, i.e. a threshold voltage regulating region "that is epitaxially grown with said conductivity type" (see VII.(a), second paragraph), the appellant's arguments relate to the way the channel including the threshold voltage regulating region (58) is made compared to the manufacturing known from D1. However, claim 1 does not concern a manufacturing method, but a device for controlling electrical conduction across a semiconductor body. Feature (d5) of device claim 1 thus merely requires that the threshold voltage regulating region is part of an epitaxially grown channel layer and has the second conductivity type. Both aspects are clearly disclosed in D1: the threshold voltage regulating region 5b is a part of epitaxially grown channel layer 5a (see D1, figure 4(c)) and is doped with the second conductivity type (see D1, figures 5(a) and 5(b)). The fact that D1 uses a different manufacturing method to obtain the same structural features is not relevant.

Moreover, the Board is not convinced that feature (d5) would improve the threshold voltage compared to the device of D1. The application as originally filed describes that the threshold voltage for a n-type grown channel layer, i.e. the one known in the art according to paragraphs [0003] and [0008] of the application as filed and lacking any p-type channel layer region, is improved by adding a p-type channel layer region acting as a threshold voltage regulating region, see paragraphs [0008], [0012] to [0015], [0032], [0037] and [0038] and see also the appellant's argumentation in the statement setting out the grounds of appeal. As the

device of D1 comprises a channel layer divided at least into four sections as claimed, it cannot be concluded that its threshold voltage is different from the claimed device. No indication can be found in the application that a further improvement of the threshold voltage compared to the device of D1 would be obtained.

From the above it follows that D1 discloses a threshold voltage regulating region "that is epitaxially grown with said second conductivity type".

4.2.3 Therefore, a device having all the claimed features is known from D1, figure 9. The subject-matter of claim 1 lacks novelty over D1 (Article 54(1) and (2) EPC).

5. Auxiliary request

According to Article 13(2) RPBA 2020 in combination with Article 25(1) RPBA 2020, any amendment to a party's appeal case made after notification of a summons to oral proceedings shall, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned.

The auxiliary request was filed after notification of the Board's summons to oral proceedings. The appellant did not indicate any reasons justifying exceptional circumstances that would have prevented it to file the auxiliary request with the statement setting out the grounds of appeal or during the examination procedure.

Moreover, feature (g) is disclosed in paragraph [0036] of the application as originally filed. However, this part of the description makes it clear that the claimed "inversion channel region" is formed when using a

retrograde profile that includes decreasing p-type carrier levels from the bottom of the P+ well (33) toward the top of the P+ well (33). Claim 1, however, is not limited to this specific type of dopant profile. According to paragraph [0037], in a device having the features mentioned in claim 1, the inversion channel region is formed only in the threshold voltage regulating region 58, see figure 2, "channel zone (50)". Thus, *prima facie*, claim 1 according to the auxiliary request does not meet the requirements of Article 123(2) EPC.

According to the above considerations, the Board does not admit the auxiliary request into the proceedings (Articles 13(2) and 25(1) RPBA 2020).

6. As not allowable request is on file, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated