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Datasheet for the decision
of 19 March 2021

Case Number: T 2531/16 - 3.4.03

Application Number: 09726572.2

Publication Number: 2260514

IPC: H01L29/808, H01L27/085

Language of the proceedings: EN

Title of invention:
A SEMICONDUCTOR DEVICE WHEREIN A FIRST INSULATED GATE FIELD EFFECT TRANSISTOR IS CONNECTED IN SERIES WITH A SECOND FIELD EFFECT TRANSISTOR

Applicant:
Eklund, Klas-Håkan

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - (no)

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Beschwerdekammern

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Case Number: T 2531/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 19 March 2021

Appellant: (Applicant)	Eklund, Klas-Håkan Manhemsvägen 20 B 191 43 Sollentuna (SE)
Representative:	Noréns Patentbyrå AB Box 10198 100 55 Stockholm (SE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 12 July 2016 refusing European patent application No. 09726572.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Ley
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 09 726 572.

II. In the decision, the following documents were cited:

D4 DE 199 02 749 A1
D5 US 5 670 393 A
D6 GB 2 013 396 A

The examining division decided that the subject-matter of claim 1 lacked novelty (Articles 52(1), 54(1) and (2) EPC) in view of the disclosure of each of documents D4, D5 and D6.

III. During the appeal procedure, the appellant submitted the following documents:

Annex 1 "Design of Digital Computers: An Introduction", Hans W. Geschwind, E. J. McCluskey, 2012, page 101

Annex 2 "Introduction to Microdisplays", D. Armitage et al., 2006

Annex 3 documentation from COMHEAT Microwave AB dated 29 January 2021

IV. The appellant requested that the decision be set aside and a European patent be granted based on the sole request (claims 1 to 8) filed during oral proceedings before the Board.

V. Claim 1 according to this request has the following wording (labelling added by the Board):

(a) A smart power semiconductor three terminal lateral device (171, 181, 19),

(b) in which a first lateral insulated gate field effect transistor (1) is connected in series with a second lateral junction field effect transistor, JFET, (2),

characterised in that

(c) the first lateral insulated gate field effect transistor (1) and the second lateral junction field effect transistor (2) being arranged in separate pockets (11, 111), and

(d) wherein both the first lateral insulated gate field effect transistor (1) and the second lateral junction field effect transistor (2) are incorporated in the surface region of a common substrate (10) and are of the same conductivity type,

(e) that a source contact terminal (171) and a gate contact terminal (181) are arranged on the first lateral insulated gate field effect transistor (1) and that a drain contact terminal (19) is arranged on the second lateral junction field effect transistor (2),

(f) that the second lateral junction field effect transistor (2) has a heavily doped source contact region (19A) which is electrically connected to a heavily doped drain contact region (191) of the first lateral insulated gate field effect transistor, and further

(g) that the breakdown voltage of the first lateral insulated gate field effect transistor (1) is higher than the pinch voltage, Vp, of the second lateral junction field effect transistor (2).

VI. The appellant provided the following arguments :

(a) D4 disclosed a vertically arranged junction field effect transistor; the normal way for the skilled person to define if a device was "vertical" or "lateral" was "the direction of the main transistor action", see the statement of grounds of appeal, page 2, first, third and fourth paragraphs.

(b) The first and second field effect transistors of D4 were not incorporated in a common substrate, because D4 disclosed an epitaxial layer 1 on top of substrate 15, see the statement of grounds of appeal, page 2, second paragraph.

(c) The device shown in D4 did not perform as a conventional JFET due to its "very long drift region (1, 2)" and its manufacturing process was "much more complex" and "more expensive" due to the epi-layer 1 and the n+ layer 2, see the statement of grounds of appeal, page 2, second paragraph.

(d) The problem solved by the invention was described on pages 1 and 2, namely to solve the problem of "integrating a high voltage and high current transistor into a combined component on a substrate together with other components as it requires a high voltage and therefore efficient cooling", see the statement of grounds of appeal, page 1, penultimate paragraph.

(e) The performance advantages of the claimed invention were outlined on page 4 of the description. With the invention it had been possible to provide a more efficient smart power device, which allowed a higher current, lower on-resistance and that

required lower power for functioning within a given area, see the letter dated 17 February 2021, page 2, penultimate paragraph and the paragraph bridging pages 2 and 3. The gate voltage could be substantially reduced and the input power for switching would be reduced.

(f) The drain - gate capacitance C_{gd} would be decreased. The MOS device would see a lower temperature by increasing the distance between the pocket with the JFET and the pocket with the MOS device. This would enhance the reliability of the device, see the letter dated 17 February 2021, page 3, second paragraph. Annex 3 also showed a 2 to 3 order advantages compared to competitive technologies.

(g) Arranging the insulated gate field effect transistor and the junction field effect transistor as lateral device in separate pockets would allow to change the size of the former compared to the latter and thus increases the freedom of design.

(h) The claimed device would provide less high voltage stress to the insulated gate field effect transistor.

Reasons for the Decision

1. The appeal is admissible.

2. The invention aims at improving a semiconductor device used in smart power applications by providing a three terminal semiconductor device having an insulated gate field effect transistor (IGFET) and a junction field

effect transistor (JFET) electrically connected in series. Both transistors are of the same conductivity type. The source and gate of the IGFET and the drain of the JFET form the three terminals. The drain of the IGFET and the source of the JFET are formed by highly doped semiconductor regions, which are electrically connected and provide a lower on-resistance compared to the known device shown in figure 1 of the application. Moreover, a better resistance against high voltages is obtained by arranging the transistors such that the breakdown voltage of the insulated gate field effect transistor is higher than the pinch voltage of the junction field effect transistor. In the claimed embodiment, both transistors are lateral devices such that they form a "semiconductor three terminal lateral device".

3. In the contested decision the examining division held that the subject-matter of claim 1 then on file lacked novelty (Articles 52(1, 54(1) and (2) EPC) in view of documents D4 to D6, see the contested decision, points 9.1, 9.2. and 9.3.

By specifying that the claimed semiconductor three terminal lateral device has a lateral IGFET electrically connected in series with a lateral JFET, the subject-matter of claim 1 is novel over D4 and D6; D4 does not disclose a lateral JFET (see section 4.2 below) and D6 only discloses lateral IGFETs connected in series (figure 1). The device shown in figures 1 and 4 of D5 showing a serial connection of an NMOS 13, a PMOS 12 and a N-channel JFET 11 is not a power device with features (f) and (g).

4. Closest prior art and distinguishing features

4.1 D4 discloses an arrangement having a lateral n-channel MOSFET (i. e. an IGFET) connected in series with an n-channel JFET in a power device, which, according to the Board's understanding, can thus be called a "smart" power device. D4 is also concerned with the problem of providing a device with a high-voltage resistance, see D4, col. 1, lines 57 to 61, "Leistungstransitor-anordnung mit hoher Spannungsfestigkeit", which corresponds to the issues dealt with in the application, see e. g. page 3, lines 15 to 23, "the compound component shall be able to resist a high voltage". Among the prior art documents at hand, only D4 solves this problem by a specific selection of the MOSFET's breakdown voltage and the JFET's pinch voltage. Thus, the Board considers that D4 is the closest prior art for assessing inventive step. This choice was not contested by the appellant.

In the wording of claim 1, Document D4 discloses a smart power semiconductor three terminal lateral device (figure 1, col. 3, line 57 to 62, "Leistungstransistor-anordnung", S, G, D), in which a first lateral insulated gate field effect transistor (n+ drain 10, channel 8, n+ source 6, gate G, 9, col. 3, lines 53 to 54, "n-Kanal MOSFET") is connected in series (figure 1, col. 2, lines 35 to 38, "monolithisch integrierte Reihenschaltung") with a second ~~lateral~~ junction field effect transistor, JFET, (n+ source 10, n region 11, drain 14, 2, gate 4, col. 3, lines 53 to 54, "JFET"), characterised in that the first lateral insulated gate field effect transistor and the second ~~lateral~~ junction field effect transistor being arranged in separate pockets (figure 1, col. 2, lines 4 to 7, "Bodyzonen 4"), and wherein both the first lateral insulated gate

field effect transistor and the second ~~lateral~~ junction field effect transistor are incorporated in the surface region of a common substrate (figure 1, p-type substrate 15, n-type epitaxial layer 1) and are of the same conductivity type (figure 1, both transistors are n-channel devices), that a source contact terminal (figure 1, "S") and a gate contact terminal (figure 1, "G") are arranged on the first lateral insulated gate field effect transistor (figure 1) and that a drain contact terminal (figure 1, "D") is arranged on the second ~~lateral~~ junction field effect transistor (figure 1), that the second ~~lateral~~ junction field effect transistor has a heavily doped source contact region (10, 11) which is electrically connected to a heavily doped drain contact region (10, 11) of the first lateral insulated gate field effect transistor (figure 1, col. 2, lines 28 to 38), and further that the breakdown voltage of the first lateral insulated gate field effect transistor is higher than the pinch voltage, Vp, of the second ~~lateral~~ junction field effect transistor (col. 2, lines 39 to 59).

4.2 The examining division considered that the device known from D4 was a lateral device with a lateral MOSFET connected in series with a lateral JFET, see point 9.1.2 of the contested decision.

The Board opines that the JFET in D4 has an up-drain-structure (col. 1, lines 1 to 11 or col. 3, lines 9 to 19), which cannot be considered as a lateral field effect transistor, although the locations of all electrodes (figure 1) are on the same side of the substrate. Despite the fact that at least a part of the current flow in JFET (10, 11, 1, 2, 14, D) is lateral (e. g. the current flow through buried region 2, col. 1, lines 4 to 9), a major part of the current flow is

vertical so that the JFET in D4 cannot be considered as lateral. As a consequence, D4 does not disclose a "semiconductor three terminal lateral device". Insofar the Board agrees with the appellant (see VI.(a) above).

4.3 Regarding the appellant's argument that the substrate in D4 was different from the claimed one (see VI.(b) above), the Board takes the view that substrate 15 with epitaxial layer 1 is to be considered as the common substrate having the first and second field effect transistors "incorporated" therein. The wording of claim 1 does not exclude a substrate having sub-parts, e. g. an epitaxial layer, see also the present application, page 5, lines 1 to 5.

4.4 The Board does not share the appellant's view that the junction field effect transistor known from D4 would not perform as a "conventional" JFET (see VI.(c) above), because it is clearly a "conventional JFET" in the sense that it was known prior to the priority date of the present application and operates in the way a JFET usually functions, as also described e. g. in D5, col. 1, lines 20 to 26. Claim 1 does not comprise any features limiting the length of the JFET's drift region so that the claimed device does not have a drift region that is necessarily shorter than the one of D4.

4.5 With respect to feature (e), the Board is of the view that the skilled person understands from D4 that the doped regions forming the source "S" and the drain "D" as well as the gate electrode "G" must be connected to the outside world via contact terminals, wherein the the term "terminal" is understood in the sense of their normal meaning in the field of semiconductor technology, see e. g. appellant's Annexes 1 and 2.

4.6 Regarding feature (f), doped n+ regions 10 in D4 are heavily doped (e. g. in comparison with regions 11 and epitaxial layer 1). Its wording also encompasses the configuration that the source region of the JFET and the drain region of the MOSFET form together a common heavily doped semiconductor region, see the wording of original dependent claim 9 in combination with the wording of original independent claim 1 (original claim 1: "the second field effect transistor (2) has a heavily doped source region (19A) which is electrically connected to a heavily doped drain contact region (191) of the first insulated gate field effect transistor", original claim 9: "the drain contact region (191) for the first insulated gate field effect transistor (1) is the same as source contact region (19A) for the second transistor device (2)").

In other words, feature (f) does not imply that the "source contact region" is of provided at a distance from the "drain contact region". Thus, feature (f) is disclosed in D4, figure 1, col. 2, lines 28 to 38 ("... wobei [...] die Drainzone des MOSFET als Sourcezone des JFET [wirkt]...").

4.7 With respect to feature (c), the Board notes that its wording does not require any distance between the pockets. It is not even excluded that the MOSFET is arranged in a first pocket, the JFET is arranged in a second pocket, wherein one of the pockets is positioned within the other one.

Moreover, claim 1 does not stipulate that the <u>entire</u> transistor is positioned within a given pocket, either, see e. g. figure 2 of the application showing a p+ and a p-base region partially outside a pocket "n-well" or page 5, lines 14 to 16 ("Within or <u>partly</u> within pocket

11, and pocket 111 a body region 12 and 121 [...] is doped ...") or page 5, lines 22 to 25 ("outside the pocket regions"). Thus the wording of claim 1 merely requires that a part of the first and second transistors is arranged within a respective pocket.

Turning to D4, col. 2, lines 4 to 7, lines 14 to 19, col. 3, lines 57 to 68 disclose a plurality of separate pockets (4) ("die unterschiedlichen Bodyzonen", "zwei benachbarte Bodyzonen", "zwei Bodyzonen"). The insulated gate field effect transistor as shown in figure 1 has its source 6, its channel 8 and a part of its drain 10 arranged within a first pocket 4 so that it is "arranged" in said first pocket 4. The junction field effect transistor has at least a part of its source and its gate formed in a second pocket 4 so that it can be said that this transistor is arranged in said second pocket. Thus, D4 discloses an arrangement within the meaning of feature (c).

4.8 It follows from the above that the subject-matter of claim 1 differs from D4 only in that the second junction field effect transistor is a lateral transistor.

5. Objective technical problem

5.1 The Board is of the view that the technical problem solved by the distinguishing feature does not correspond to the various problems indicated by the appellant (see sections VI.(d), (e), (f) and (h) above).

The disadvantages of the prior art as indicated on page 1, line 27 to page 2, line 5, are overcome by a device having the features of claim 1 as originally filed,

i. e. features (f) and (g), see the application, page 2, lines 7 to 15. As the semiconductor device known from D4 has both features, the integration problem mentioned by the appellant is already solved. Page 1, line 27 to page 2, lines 15 also make it clear that a device having features (f) and (g), i. e. the one known from D4, allows "a higher current", "lower on-resistance" and "requires lower power for functioning within a given area".

The effects mentioned on page 4, lines 1 to 7 (i. e. a higher input capacitance and a lower gate voltage) are obtained when the width of the insulated gate field effect transistor is made larger than the width of the junction field effect transistor, i. e. by features which are not a part of claim 1.

The effect mentioned on page 4, lines 9 to 13 is already obtained in D4 by the fact that there is no overlap between gate G, 9 and drain 14 in the device of figure 1. Claim 1 does not comprise any features which would imply that the drain-to-gate capacitance C_{gd} in the claimed device is necessarily smaller than that of the device known from D4. As already noted in section 4.7 above, the wording of feature (c) does not imply any distance between the respective pockets.

The effect mentioned on page 4, lines 15 to 22 (i. e. a better resistance to high voltage stress) is already obtained in D4 by feature (g), see also D4, col. 2, lines 39 to 53.

With respect to Annex 3, the Board notes that it apparently concerns a device using the invention and "further developed" by the company Comheat, see appellant's letter dated 17 February 2021, page 3,

third and fourth paragraphs. There is no indication that Annex 3 compares a device according to claim 1 and D4. A possible technical effect solved by the distinguishing features of claim 1 compared to the device known from D4 cannot be derived thereof.

5.2 The Board is of the view that the manufacturing of the device of D4 does not necessarily imply an increased complexity and higher manufacturing costs compared to the claimed device due to the fact that a substrate with an epitaxial layer is used, see section VI.(c) above. This type of substrate is not excluded by the wording of claim 1, see section 4.3 above.

5.3 Finally, with respect to the argument of section VI.(g) above, the Board points out that the wording of claim 1 requires neither a distance between the pockets nor between the highly doped source and drain contact regions, see sections 4.6 and 4.7 above. Therefore, the Board is not convinced by the appellant's argument made during oral proceedings, that the claimed device would necessarily provide a "separation of the devices" and thus a "design freedom", e. g. the possibility to change the size of the insulated gate field effect transistor independently from the junction field effect transistor. Even for the power semiconductor device of D4 the skilled person has the "freedom" to change the design and/or size of the MOSFET independently of the JFET by choosing a proper arrangement of the various doped parts (4, 6, 10, 11).

5.4 As the application as originally filed is silent about any technical problem solved by the distinguishing feature and as the appellant's arguments could not convince the Board, it seems justified to formulate the objective technical problem in a broader way, namely

how to provide an alternative arrangement for the JFET in D4.

6. Obviousness

The skilled person knows from its common general knowledge or from D5 (figure 4) that an alternative arrangement for the JFET of D4 is a lateral JFET. D5 discloses the integration of a lateral n-channel MOSFET 420 with a lateral n-channel JFET 430 on a common substrate 400, wherein each transistor is arranged in its own pocket 421, 431 separated by elements 440, see D5, col. 4, lines 23 to 31, col. 4, line 65 to col. 6, line 6, figure 4.

In order to solve the objective technical problem, it is obvious for the skilled person to replace the JFET of D4 by the lateral JFET already known from D5. In other words, the subject-matter of claim 1 lacks an inventive step over D4 in combination with D5.

7. As no allowable set of claims is on file, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

S. Sánchez Chiquero

G. Eliasson

Decision electronically authenticated