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Datasheet for the decision of 10 March 2022

Case Number: T 2641/16 - 3.4.03

Application Number: 11749962.4

Publication Number: 2641270

IPC: H01L25/065, H04L12/56, G06F15/78, H01L23/14, H01L23/538

Language of the proceedings: EN

Title of invention:
MULTICHIP MODULE FOR COMMUNICATIONS

Applicant:
Xilinx, Inc.

Relevant legal provisions:
EPC Art. 52(1), 54(1), 54(2), 56, 84
EPC R. 46(2)(h)

Keyword:
Inventive step - main request (yes)
Claims - support in the description (yes)

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Beschwerdekammern

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Case Number: T 2641/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 10 March 2022

Appellant: Xilinx, Inc.
(Applicant) 2100 Logic Drive
San Jose, California 95124 (US)

Representative: Gibbs, Richard
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 20 July 2016 refusing European patent application No. 11749962.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman T. Häusser
Members: M. Ley
G. Decker

Summary of Facts and Submissions

I. The appeal lies from the decision of the examining division to refuse European patent application No. 11 749 962 pursuant to Article 97(2) EPC.

II. The examining division decided that none of the claims according to the main request or to the auxiliary requests 1 to 4 involved an inventive step within the meaning of Article 56 EPC.

The following documents were cited in the contested decision:

D1 US 6 721 313 B1
D2 XP002448786
D3 XP011252830
D6 US 2006/237835 A1
D7 XP002438746
D8 XP031692661

III. The appellant requests that the contested decision be set aside and a patent be granted on the basis of the set of claims according to the main request or according to the first to fourth auxiliary requests underlying the decision and re-filed with the grounds of appeal.

With the statement of grounds of appeal the appellant re-filed a written "Declaration" by Mr Ephrem C. Wu that it had already submitted to the examining division prior to the oral proceedings.

The appellant requests oral proceedings "to allow the Applicant a chance to be heard before any final

decision is issued" in the "event that the Board consider that any objections still require to be addressed".

IV. In a first communication pursuant to Rule 100(2) EPC, the Board informed the appellant of its opinion that the claims of the main request met the requirements of the EPC and that the description should be adapted to the set of claims according to the main request.

With its letter dated 20 October 2021, the appellant filed amended description pages 1 to 18 and with the letter dated 8 December 2021 it filed amended description pages 4, 5, 8, 9, 11, 14 to 17 and a set of drawing sheets 1/10 to 10/10.

V. The appellant requests therefore as a main request that the decision under appeal be set aside and the case be remitted to the department of first instance with the order to grant a European patent in the following version:

- Claims:
No. 1 to 13 according to the main request filed with the statement setting out the grounds of appeal dated 29 November 2016;

- Description:
Pages 1 to 3, 6, 7, 10, 12, 13 and 18 filed with the letter dated 20 October 2021 and pages 4, 5, 8, 9, 11, 14 to 17 filed with the letter dated 8 December 2021;

- Drawings:
Sheets 1/10 to 10/10 filed with the letter dated 8 December 2021.

VI. Claim 1 according to the main request has the following wording:

A multichip module (500), comprising:
a first transceiver die (501-1) having first transceivers (511);
a second transceiver die (501-2) having second transceivers (511);
a crossbar switch die (503) having at least one crossbar switch (513);
a first protocol logic blocks die (502-1) having first protocol logic blocks (512);
a second protocol logic blocks die (502-2) having second protocol logic blocks (512); and
a silicon interposer (510) to which the first transceiver die, the second transceiver die, the crossbar switch die, the first protocol logic blocks die, and the second protocol logic blocks die are coupled;
wherein the first and second transceiver dice, the first and second protocol logic blocks dice, and the crossbar switch die are mounted on the interposer; and wherein the interposer interconnects the first transceivers and the first protocol logic blocks to one another, interconnects the second transceivers and the second protocol logic blocks to one another, interconnects the first protocol logic blocks and the at least one crossbar switch to one another, and further interconnects the second protocol logic blocks and the at least one crossbar switch to one another.

Claim 9 according to the main request has the following wording:

A method (1200) for communication, comprising:
receiving (1201) a packet (1125) by a first transceiver die (501-1) of a multichip module (500);

providing (1202) the packet from the first transceiver die to a first protocol logic blocks die (502-1) of the multichip module via a silicon interposer (510);
wherein the interposer interconnects the first transceiver die and the first protocol logic blocks die to one another;
providing (1203) the packet from the first protocol logic blocks die to a crossbar switch die (503) of the multichip module via the interposer;
wherein the interposer interconnects the first protocol logic blocks die and the crossbar switch die to one another;
providing (1204) the packet from the crossbar switch die to a second protocol logic blocks die (502-2) of the multichip module via the interposer;
wherein the interposer interconnects the second protocol logic blocks die and the crossbar switch die to one another;
providing (1205) the packet from the second protocol logic blocks die to a second transceiver die (501-2) of the multichip module via the interposer;
wherein the interposer interconnects the second protocol logic blocks die and the second transceiver die to one another; and
sending (1206) the packet from the second transceiver die out of the multichip module.

Reasons for the Decision

1. The appeal is admissible.

2. The invention concerns a multichip module for communications having first and second transceiver dice, first and second protocol logic blocks dice and a crossbar switch die, all five dice being mounted on a

silicon interposer that provides the required electrical connections.

3. Claim 1 according to the main request is based on claims 1 and 2 as originally filed and claim 9 is based on claims 10 and 11 as originally filed, wherein for both independent claims it has been specified that the "interposer" is a "silicon interposer", based on page 14, lines 30 and 31, page 15, line 12, page 17, lines 9 to 11, and page 18, lines 1 to 14.

The Board is satisfied that the requirements of Article 123(2) EPC are met.

4. Inventive step - Article 56 EPC

4.1 The examining division considered document D1 as the closest prior art.

The examining division identified conductive traces on or in the substrate of the chip known from D1 (column 3, lines 53 to 55, "single die") as an "interposer" and held that the subject-matter of claim 1 differed from the chip of D1 in that the "interposer" was a silicon interposer and that the first and second transceiver "blocks", the crossbar switch "block", and the first and second protocol logic "blocks" were implemented in dedicated, respective dice and assembled together in a multichip module, wherein the dice are not only coupled to the interposer, but mounted on it, see the contested decision, sections 18.1 and 18.2.

The examining division held that, in view of the distinguishing features, the objective technical problem was to find "an alternative implementation of a

network processor in view of the new technological and/ or economical considerations, i.e. a routine problem", see the contested decision, section 18.3. It was common general knowledge that an electronic system could be integrated at different levels (board-level integration, package-level integration ("system-in-package", "SiP") or chip-level-integration ("system-on-chip", "SoC"). Knowing the advantages and disadvantages of the different integration levels (e.g. from D2, pages 192 to 193, chapter 6.2 or from D3) and knowing that any electronic circuit could be "divided into modules and fabricated as a multi-chip module having multiple dice, all mounted on a silicon interposer", the skilled person would implement the die of D1 as a multi-chip module, see the contested decision, section 18.5. For the examining division, the skilled person would split up the switch fabric design into multiple modules in the way required by claim 1. Since the architecture of the switch fabric in itself was a modular one, the person skilled in the art would use different, distinct dice for the different logical blocks of the switch fabric and would "cut" a given modular design along existing interfaces of the modules of the modular design, see the contested decision, section 18.6.

4.2 The appellant argued that in D1 every component of the integrated switch fabric architecture was provided on a single, common die, contrary to the multichip module of claim 1 of the main request. D1 did not disclose an interposer, let alone a silicon interposer. According to D1, abstract, claim 1, column 1, lines 51 to 56, column 2, lines 17 to 51, column 3, line 53 to 55, its components of Figure 1 were "all simply provided on a single die" and not as an arrangement of "separated

'blocks' of components that would correspond to separate dice".
The appellant argued that the purpose of the arrangement of D1 was to maximally integrate two different SERDES transceiver type cores on a single die, see e.g. abstract, claim 1, column 1, lines 51 to 56, column 2, lines 17 to 51, column 3, lines 53 to 55. If a skilled person were instead looking to provide a switch fabric architecture on multiple dice then they would start from a different prior art system and would not implement the features of D1, as it would be counter-intuitive to incorporate features aimed at maximising integration of different transceiver types on a single die when the skilled person’s goal is to provide a dispersed system spread over multiple dice.

For the appellant, nothing in the prior art would clearly and unambiguously lead a skilled person to the features of claims 1 and 9 of the main request, "at least without the unallowable benefit of hindsight". D1 addressed the object of increasing integration in a monolithic single IC chip die and a skilled person would "not take the very opposite direction" by providing a multichip module according to D2, D3, D7 or D8; none of these documents concerned communication switches. There was also no teaching that the switch module of D1 could be implemented in the way required by claim 1, i.e. by using five dice interconnected in the claimed manner and mounted on a silicon interposer. The technical problem solved by the claimed arrangement was to provide switch modules that were easier and cheaper to manufacture (see the application, page 9, lines 15 to 27, page 13, line 28 to page 14, line 16).

4.3 The Board agrees with the appellant that the subject-matter of independent claims 1 and 9 does involve an inventive step for the following reasons.

4.3.1 Closest prior art

Since the examining division and the appellant used D1 as the closest prior art and since even the application as originally filed mentions a device on a single chip (see page 1, lines 9 to 16, "conventionally ... formed of a single monolithic integrated circuit") as the background art the present invention aims to improve, the Boards accepts to use D1 as the closest prior art.

4.3.2 Distinguishing features

The Board opines that D1 does not disclose an entity that a person skilled in the art would consider an "interposer", contrary to the examining division's view. It seems undisputed that the chip of D1 discloses a substrate and conductive traces on or in the substrate of the chip for connecting elements 12a to 12d, 15a to 15d, 25, 35a to 35n, 32a to 32n as shown in Figure 1. The Board, however, disagrees with the examining division that these conductive traces should be considered an "interposer".

The Board further takes the view that components 12a to 12d, 15a to 15d, 35a to 35n, 32a to 32n each have their specific function in the integrated switch fabric architecture of Figure 1 and can therefore be regarded as "blocks".

Thus, in the wording of claim 1 of the main request, D1 discloses a ~~multichip module~~ single die (Figure 1), comprising:

a first transceiver ~~die~~ block (column 3, line 62 to column 4, line 7) having first transceivers ("array of ICC SERDES Transceiver (XCVR) Cores 12a, . . . 12d", Figure 1);
a second transceiver ~~die~~ block (column 3, line 62 to column 4, line 7) having second transceivers ("an array of HSB SERDES XCVR Cores 32a, 32d, . . . 32n", Figure 1);
a crossbar switch ~~die~~ block (25, column 3, line 62 to column 4, line 7) having at least one crossbar switch ("a Crossbar Switch 25");
a first protocol logic blocks ~~die~~ (column 3, line 62 to column 4, line 7) having first protocol logic blocks ("array of ICC Protocol Translators 15a, . . . , 15d", Figure 1);
a second protocol logic blocks ~~die~~ (column 3, line 62 to column 4, line 7) having second protocol logic blocks ("array of HSB Protocol Translators 35a, 35d, . . . , 35n", Figure 1); and
a ~~silicon interposer~~ connecting means (Figure 1) to which the first transceiver ~~die~~ block, the second transceiver ~~die~~ block, the crossbar switch ~~die~~ block, the first protocol logic blocks ~~die~~, and the second protocol logic blocks ~~die~~ are coupled;
~~wherein the first and second transceiver dice, the first and second protocol logic blocks dice, and the crossbar switch die are mounted on the interposer; and~~
wherein the ~~interposer~~ connecting means interconnects the first transceivers and the first protocol logic blocks to one another, interconnects the second transceivers and the second protocol logic blocks to one another, interconnects the first protocol logic blocks and the at least one crossbar switch to one another, and further interconnects the second protocol logic blocks and the at least one crossbar switch to one another (Figure 1).

In view of the above considerations, the difference between the subject-matter of claim 1 and the switch fabric architecture 10 of D1 is the device implementation. In D1, a single common die is used, whereas, according to claim 1, a multichip module having five dice on a silicon interposer is used.

4.3.3 Objective technical problem

The Board understands from sections 18.3 and 18.5, in particular from the last paragraph of page 9, of the contested decision that for the examining division the objective technical problem solved by the invention was to provide the advantages of a system-in-package, namely a modular design, high bandwidth, higher wiring density, for the switch fabric architecture of D1.

The appellant argued that the objective technical problem to be solved was to reduce the costs and simplify the manufacturing compared to high-throughout switch fabric integrated circuits on a single monolithic IC as known from D1, see the statement of grounds of appeal, page 6, second paragraph and the application as originally filed, page 1, lines 9 to 16, page 9, lines 15 to 27, page 13, line 28 to page 14, line 16 and also Mr Wu's "Declaration", page 3, first paragraph.

The Board is not convinced that the features of claim 1 would necessarily provide a higher bandwidth or wiring density in comparison with D1. The claimed multichip module, however, allows "modular design" and, thereby, implementing the marketing strategy "make-to-order". For the Board, the modular design would necessarily result in a simplified manufacturing, as argued by the appellant, because each component is made independently

according to its own requirements and then mounted on a silicon interposer. The objective technical problem is therefore to modify the switch fabric of D1 to facilitate its manufacturing.

4.3.4 Obviousness

The Board agrees with the examining division that at the priority date of the present application an interposer carrying multiple chips to form a multichip module (or system-in-package, SiP) was known to the skilled person, see D7, Figure 2 or D3 for silicon interposers, D2 for organic interposers, D6, [0089] for glass interposers. The Board agrees that the advantages, such as modular design, high bandwidth or higher wiring density, related to this type of module compared to a system-on-chip (SoC) are known to the skilled person from D7.

The Board is however not convinced that in principle any electronic circuit could be "divided into modules and fabricated as a multi-chip module", as argued in the contested decision in sections 16.5 and 18.5, but it accepts that the electronic circuit of D1 could be implemented as a multi-chip module.

The question, however, if the skilled person would build the SoC device of D1 as SiP, must be answered in the negative.

The purpose of D1 is clearly to provide on a single monolithic die:

- an array of ICC SERDES Transceiver (XCVR) Cores,

- a corresponding array of ICC Protocol Translators with each ICC Protocol Translator connected with a corresponding ICC Transceiver Core,
- an array of HSB SERDES XCVR Cores,
- a corresponding array of HSB Protocol Translators with each HSB Protocol Translator connected with a corresponding ICC Transceiver Core,
- a Crossbar Switch interfaced with each ICC Protocol Translator and HSB Protocol Translator device,

see e.g. column 1, lines 8 to 14, lines 51 to 56, column 2, lines 17 to 51, column 3, lines 51 to 61, column 4, lines 8 to 64, claim 1, Figure 1. D1 also states that the single die is a modular element, see e.g. column 3, line 56 and 57, to be used in building a switch fabric. The skilled person is taught away from providing the different components of Figure 1 as individual dies and implementing the circuit shown in Figure 1 as a multichip module. The skilled person wishing to solve the objective technical problem would rather consider other solutions to simplify the manufacturing of the single die of D1, instead of considering the solution of claim 1.

Even if the skilled person were to consider the teaching of D7 and implement the circuit of D1 as a multichip module with a silicon interposer, there is no indication in the prior art at hand that it would select the specific modular design of claim 1. The Board does not follow the examining division's argument of section 18.6 of the contested decision that the skilled person would "cut" a given modular design along existing interfaces of the modules of the modular design. The skilled person could provide a multichip arrangement as claimed or they might provide the ICC SERDES XCVR Cores 12a to 12d and their corresponding

array of ICC Protocol Translators 15a to 15d on one die and/or the HSB SERDES XCVR Cores 32a to 32n and their corresponding array of HSB Protocol Translators 35a to 35n on one die, i.e. use three or four dice on a silicon interposer. There is no indication in the prior art at hand that the skilled person would select five dice mounted on a same silicon interposer as required by claim 1.

Hence, the subject-matter of claim 1 is not rendered obvious by a combination of D1 with any of D2, D3 or D7 and involves an inventive step (Article 56 EPC).

For the same reasons, the subject-matter of claim 9 involves an inventive step.

5. Adaptation of the description, renumbering of the figures

The appellant deleted from the description the examples not falling under the scope of claims 1 and 9. Any inconsistencies between the wording of the claims have been removed. The Board is thus satisfied that the claims are supported by the description as required by Article 84, second sentence, EPC.

By renumbering the figures consecutively, the requirements of Rule 46(2)(h) EPC are also fulfilled.

6. As the set of claims according to the main request meets the requirements of the EPC, there is no need to examine the auxiliary requests. It is not necessary to hold oral proceedings, either.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a European patent in the following version:

   Claims:
   No. 1 to 13 according to the main request filed with the statement setting out the grounds of appeal dated 29 November 2016;

   Description:
   Pages 1 to 3, 6, 7, 10, 12, 13 and 18 filed with the letter dated 20 October 2021 and pages 4, 5, 8, 9, 11, 14 to 17 filed with the letter dated 8 December 2021;

   Drawings:
   Sheets 1/10 to 10/10 filed with the letter dated 8 December 2021.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Häusser

Decision electronically authenticated