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Datasheet for the decision of 12 November 2021

Case Number: T 0328/17 - 3.4.03

Application Number: 06799911.0

Publication Number: 1886352

IPC: H01L29/267, H01L29/778, H01L21/335, H01L21/84, H01L21/20, H01L21/18

Language of the proceedings: EN

Title of invention:
GALLIUM NITRIDE MATERIAL STRUCTURES INCLUDING SUBSTRATES AND METHODS ASSOCIATED WITH THE SAME

Applicant:
MACOM Technology Solutions Holdings, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - all requests (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 0328/17 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 12 November 2021

Appellant: (Applicant)	MACOM Technology Solutions Holdings, Inc. 100 Chelmsford Street Lowell, Massachusetts 01851 (US)
Representative:	Moore, David Simon Jensen & Son 366-368 Old Street London EC1V 9LT (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 15 September 2016 refusing European patent application No. 06799911.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Stenger
	E. Mille

Summary of Facts and Submissions

I. The appeal concerns the decision of the Examining Division to refuse European patent application No. 06799911. In the contested decision, the Examining Division set out that the independent claims of the main request then on file did not meet the requirements of Articles 123(2), 84 and 56 EPC. Objections relating to the same Articles were raised for the independent claims of the auxiliary request then on file.

In a section titled "Additional observations", further comments concerning Article 84 were made with respect to the independent claims and some dependent claims of all requests. Moreover, objections under Article 56 EPC with respect to the dependent claims of all requests were discussed.

II. The appellant requested (grounds of appeal, pages 1 and 2) that the contested decision be set aside in its entirety and that a patent be granted on the basis of a main request or a first or a second auxiliary request, all filed with the grounds of appeal. For the case that the main request was not allowed, the appellant initially requested that oral proceedings be appointed, but withdrew this request with letter dated 6 July 2021. Consequently, the scheduled oral proceedings were cancelled.

III. It is referred to the following documents:

D1: PHILIPPE A. ET AL.: "PHOTOLUMINESCENCE CHARACTERISTICS OF GaN LAYERS GROWN ON SOI SUBSTRATES AND RELATION TO MATERIAL PROPERTIES", Materials Research Society Symposium Proceedings, Materials

Research Society, Pittsburg, PA, US, vol. 482, 5 December 1997, pages 307-312, XP009077706

D2: KIPSHIDZE g. et al.: "High Quality AlN and GaN Grown on Compliant Si/SiC Substrates by Gas Source Molecular Beam Epitaxy", Journal of ELECTRONIC MATERIALS, Vol. 30, Noo. 7, July 2001, pages 825-828, XP009077717

D3: US 2005/082563 A1

D5: WOLF S ED - STANLEY WOLF: "Chap. 11 Silicon-on-Insulator (SOI) Technology", SILICON PROCESSING FOR THE VLSI ERA - VOL. 4 DEEP-SUBMICRON PROCESS TECHNOLOGY; LATTICE PRESS, US, 2002, pages 501-572, XP009112914

D6: S.Q.Zhou et al.: "Comparison of the properties of GaN grown on complex Si-based structures", Appl. Phys. Lett. 86, 081912 (2005), published online 16 February 2005

D6 was introduced by the Board in its communication preparing the oral proceedings. A copy of the document was attached to that communication.

IV. Claim 1 of the main request is worded as follows (labelling a), b), ... added by the Board):

a) *A gallium nitride material semiconductor structure (10) comprising:*
b) *a composite substrate (12) comprising a silicon surface layer (14) having a thickness of between 0.1 micron and 10.0 microns, and a lower portion (16) having at least two layers and a thickness of greater than 100 microns,*

c) *wherein the composite substrate has a diameter of between 100 mm and 400 mm;*
d) *a gallium nitride material region (22) formed over the composite substrate having a thickness of greater than 2.0 microns;*
e) *wherein the silicon surface layer (14) is formed on the lower portion (16)*
f) *and absorbs strain associated with formation of the gallium nitride material region (22).*

V. Claim 1 of the first auxiliary request differs from claim 1 of the main request in that feature d) is replaced by feature d') and in that it comprises, between features c) and d'), additional feature g) as follows (labelling d'), g) added by the Board):

g) *an amorphous strain-absorbing layer formed on the composite substrate and having a thickness greater than 0.001 microns and less than 0.01 microns;*

d') *a gallium nitride material region (22) formed over the strain absorbing layer and having a thickness of greater than 2.0 microns;*

and in that the word "of" is deleted between "thickness" and "greater" in the last expression of feature b).

VI. Claim 1 of the second auxiliary request differs from claim 1 of the first auxiliary request in that feature b) is replaced by feature b') and in that it comprises, at its end, additional feature h) as follows (labelling b'), h) added by the Board:

b') *a composite substrate (12) comprising a crystalline silicon surface layer (14) having a*

thickness of between 0.1 micron and 10.0 microns, and a lower portion (16) on which the surface layer is formed, the lower portion having a thickness greater than at least 10 times the thickness of the silicon layer and greater than 100 microns,

h) *wherein the lower portion comprises polycrystalline material.*

VII. The arguments of the appellant are referred to in detail in the section Reasons for the Decision below.

Reasons for the Decision

1. The appeal is admissible.

2. Main request

2.1 D1

D1 is a scientific article relating to MOCVD growth of GaN layers on Silicon-on-Insulator substrates aiming at improving the GaN material quality as compared to sapphire substrates. The compliant growth of GaN on SOI substrates leads to lower strain in the layers (see abstract).

In the wording of claim 1 of the main request, D1 discloses

a) A gallium nitride material semiconductor structure (see abstract) comprising:
b)(part) a composite substrate ("SOI") comprising a silicon surface layer ("silicon overlay", page 307, last line), and a lower portion having at least two layers (an SiO_2 buried layer created by a SIMOX process

and the bulk silicon portion below the buried layer, page 307, last paragraph),
d) a gallium nitride material region ("GaN") formed over the composite substrate having a thickness of greater than 2.0 microns (see table I, sample B);
e) wherein the silicon surface layer is formed on the lower portion
f) and absorbs strain associated with formation of the gallium nitride material region (see abstract: "suggests the presence of lower strain in the layers which is expected for compliant growth on SOI substrates").

2.2 Closest prior art

In the contested decision, D1 was regarded as being the closest prior art. The appellant did not object.

D1 is directed at the same objective as the present application, namely, to provide a Gallium Nitride semiconductor structure, and shares most of the relevant technical features therewith, that is providing a Gallium Nitride material region on top of a composite substrate having a silicon surface layer and a lower portion (see above).

Thus, D1 is a suitable starting point for the problem solution approach.

2.3 Difference

Claim 1 of the main request differs from D1 only in the dimensions defined in features b) and c), namely in that

i) the silicon surface layer has a thickness of between 0.1 micron and 10.0 microns
ii) the lower portion has a thickness of greater than 100 microns, and in that
iii) the composite substrate has a diameter of between 100 mm and 400 mm.

These distinguishing features correspond essentially to the ones identified by the Examining Division in the contested decision (see point II.3.2) for claim 1 of the main request as then on file; only one of the distinguishing features identified by the Examining Division has been deleted from the claim to overcome an objection relating to Article 84 EPC.

2.4 Objective technical problem

The Examining Division regarded the objective technical problem as "how to provide an alternative compliant substrate". The appellant did not contest this choice and the Board sees no reason to disagree.

2.5 Inventive step, arguments of the appellant

The Examining Division argued, referring to D5 for documenting the common general knowledge, that the dimensions for the thicknesses and the diameter defined in distinguishing features i) to iii) included values commonly used for composite substrates (see point II. 3.4 of the contested decision).

The submissions of the appellant with respect to the inventive step objections concerning the main request relate to distinguishing feature i) only (see statement of grounds of appeal, points 11 to 34).

The Board concurs with the Examining Division that the dimensions for the thickness of the lower portion and the diameter of the substrate defined in distinguishing features ii) and iii) comprise values commonly used for composite substrates.
Since the appellant did not contest this finding during the appeal procedure, it is not necessary to further discuss that issue.

2.5.1 Concerning feature i), the appellant submitted that D5, when considered in its entirety, pointed to silicon layer thicknesses below 50 nm, i.e. below the lower limit defined in feature i) (see statement of grounds of appeal, points 14 to 25).

D5 discloses that the market segment of thick SOI-MOSFETS is much smaller than the market segment of thin SOI-MOSFETS. That is said to be the reason why D5 focuses on thin SOI devices with a silicon layer thickness of 0.005 to 1 micron.
The skilled person would nevertheless learn from D5 that SOI devices with silicon layer thicknesses of more than 1 micron were commonly used before 2002 (see page 518).

Further, even for the case of thin SOI devices, 95% of the thickness range disclosed in D5 overlaps the thickness range defined in feature i). Particular examples with silicon layer thicknesses of 0.1 micron to 0.2 microns are given as well (see figure 11-8).

Thicknesses for the silicon layer outside the range defined in feature i) are disclosed in D5 only for the specific case of fully depleted SOI MOSFETS (see page 523 and figure 11-13 of D5).

On the other hand, D5 discloses that the silicon layers produced by a SIMOX process are typically 150 to 250 nm thick (page 530; see also table 11-3). The only thinner silicon layer produced using a SIMOX process mentioned in D5 has been further thinned *after* the SIMOX process proper (see section 11.5.3.1).

To summarize, D5 discloses that typical silicon layers produced by a SIMOX process are well in the range defined by feature i). D5 mentions a plurality of devices where structures with such a silicon layer thickness are actually used. Silicon layers with a thickness below the lower limit defined in feature i) are indicated to be desirable only for a very particular type of semiconductor device, namely fully depleted SOI-MOSFETS.

Thus, D5 does not point to silicon layers below 50 nm, contrary to the arguments of the appellant.

2.5.2 The appellant further submitted that D5, which was published in 2002, could not be used as evidence of the common general knowledge in 2005 (statement of the grounds of appeal, points 26 to 28).

The Board accepts that SOI technology was evolving between 2002 and 2005. However, a textbook like D5 published in 2002 will normally be part of the common general knowledge of the skilled person not only in its year of publication, but also in the years thereafter. Thus, D5 can be used as evidence for the common general knowledge in 2005, contrary to the argument of the appellant.

2.5.3 In addition, the appellant argued that the thickness of the silicon layer of 53 nm disclosed in D1 was a

standard thickness and the skilled person would not have thought to use thicker silicon layers, in particular since the trend in industry was moving towards thinner silicon layers (statement of grounds of appeal, points 29 to 32).

However, as evidenced by D5, typical standard thicknesses of the silicon layer in a SIMOX-produced SOI were around 0,15 microns to 0,25 microns (see above). Since it is always beneficial to use standard components in terms of availability and cost, the skilled person, starting from D1, would have had a reason to use silicon layers thicker than 53 nm, contrary to the argument of the appellant.

The move towards thinner silicon layers mentioned by the appellant is restricted to particular semiconductor devices (as mentioned above), whereas the application is not restricted to any such particular semiconductor device.

2.5.4 Finally, the appellant submitted that the fact that the solution of D1 had not been improved during the 7 years up to 2005 was a secondary indicator of the presence of inventive step (statement of grounds of appeal, point 34)

The Board notes that D6, which was published in February 2005 shortly before the priority date of the present application, discloses GaN material of good quality grown on SOI the top silicon layer of which has a thickness of 200 nm (see abstract and first page, left-hand column, last paragraph). GaN was thus grown on SOI with a silicon layer thickness falling into the range defined in feature i), contrary to the argument of the appellant.

2.5.5 Inventive step

For the above reasons, the Board does not accept the arguments of the appellant.
Instead, the Board is convinced that the skilled person, starting from D1 and being confronted with the problem of providing an alternative compliant substrate, would readily have chosen, as a matter of routine design, dimensions commonly used in the art. In that manner, they would have arrived at dimensions falling into the ranges defined in distinguishing features i), ii) and iii).
Thereby, they would have arrived at the subject-matter of claim 1 of the main request without the exercise of an inventive step under Article 56 EPC 1973, as set out in the contested decision (see points II.3.3 and II. 3.4).

3. First auxiliary request

Independent claim 1 of the first auxiliary request includes the additional feature g) that the semiconductor further comprises:

g) an amorphous strain-absorbing layer formed on the composite substrate and having a thickness greater than 0.001 microns and less than 0.01 microns;

the gallium nitride region then being formed over this strain absorbing layer according to feature d').

Additional feature g) is not disclosed in D1 and thus constitutes a further distinguishing feature, as noted by the Examining Division (point II.8.1 of the contested decision) and the appellant (statement of the

grounds of appeal, point 41). The Examining Division argued that the problem solved by this additional feature was independent of the problem to provide an alternative substrate and that the subject-matter of claim 1 of the first auxiliary request was not inventive in view of D1 combined with D3 and the common general knowledge (see contested decision, points II. 8.2 to II.8.4).

The appellant submitted that D1 already reduced stress by using a compliant structure. Starting from D1, the skilled person would not have used more than one arrangement for reducing stress and would therefore not have thought of using the stress absorbing layer of D3 in addition to the compliant substrate of D1 (statement of grounds of appeal, points 45 to 47).

However, the Board is of the opinion that the skilled person would always try to further enhance the thickness and crystalline quality of the device layer of a semiconductor structure, contrary to the arguments of the appellant.

Further, in the present case and as noted by the appellant, D1 discloses that the use of a compliant SOI substrate is beneficial for growing GaN layers as compared to using a sapphire substrate (statement of the grounds of appeal, point 44). The skilled person would nevertheless have realized that using such an SOI substrate for GaN growth would result in an Si - GaN interface at the top layer of the substrate involving a large lattice mismatch.

That is, in the present case, the skilled person would even have had a particular interest in searching for possibilities to mitigate the influence of this

mismatch, contrary to the arguments of the appellant. D3 relates to that problem (see paragraphs [14] to [16]) and suggests to form an amorphous strain-absorbing layer (see paragraph 65, "amorphous silicon nitride layer 721") with a thickness on the substrate (see paragraph [65], "best preferably of 10 Å - 30 Å.") falling into the range between 0.001 microns/10 Å and 0.01 microns/100 Å as required by feature g), before depositing a GaN layer as required by feature d').

The skilled person would thereby, starting from D1 and using the teaching of D3 as well as their common general knowledge, have arrived at the subject-matter of claim 1 of the first auxiliary request without the exercise of an inventive step under Article 56 EPC 1973, as concluded by the Examining Division (point II. 8.4).

4. Second auxiliary request

4.1 Closest prior art, differences

The independent claims of the second auxiliary request are directed at a semiconductor structure with a different lower portion of the composite substrate than the independent claims of the preceding requests. In particular, as defined in features b') and h), the lower portion of the composite substrate according to the independent claims of the second auxiliary request has a thickness greater than at least 10 times the thickness of the silicon layer and comprises polycrystalline material.

Contrary to D1, D2 discloses a substrate with a lower portion comprising polycrystalline material. It is thus more appropriate to regard D2, which discloses a

Gallium Nitride material region on top of a composite substrate having a silicon surface layer and a lower portion comprising polycrystalline material, as closest prior art for the subject-matter of claim 1 of the second auxiliary request. D2 was discussed by the Examining Division in section "III. Additional observations" of the contested decision (see point III. 3).

Claim 1 of the second auxiliary request differs from D2 (see section "Introduction" and the left-hand column of page 827) by feature g) as defined above and by features ii') and iv) as follows:

ii') the lower portion has a thickness at least 10 times the thickness of the silicon layer and greater than 100 microns,

iv) the gallium nitride material region has a thickness of greater than 2.0 microns.

As a side remark, the Board notes that according to the only example comprised in the application (page 23, line 24 to page 24, line 8), the strain-absorbing layer has no defined lower thickness limit and the thickness of the GaN material region is about 1.7 microns. That is, the dimensions of the only example disclosed in the application do not fall within the ranges defined by claim 1 of the second auxiliary request.

4.2 Features ii') and iv)

In its communication preparing the oral proceedings, the Board found that distinguishing features ii') and iv), which like features i), ii) and iii) relate to dimensions of the semiconductor structure, were mere

design options which the skilled person would have chosen according to the circumstances without the exercise of an inventive step. The appellant did not submit any argument contrary to this finding. It is thus not necessary to delve into that issue further.

4.3 Feature g)

Instead, the submissions of the appellant pertained to feature g). They argued that D3 explained that when GaN was deposited on Si, most of the GaN took the form of crystalline pillars and the stress resulting from the different lattice constants caused cracking of the GaN epitaxy layer. D2, on the other hand, already suggested a solution of eliminating cracking of the GaN by using a thin silicon layer resulting in initial relaxation of an AlN buffer layer. Thus, starting from D2, the skilled person would not have considered modifying D2 to provide a stress absorbing layer as taught by D3 (see statement of grounds of appeal, points 57. to 62.).

The Board accepts that D2 discloses that no cracking was observed for 0.5 microns thick GaN layers (right-hand column of page 826). However, as mentioned above with respect to the first auxiliary request, the skilled person would always try to further enhance the thickness and crystalline quality of the device layer of a semiconductor structure, contrary to the arguments of the appellant.

Further, in the present case, D2 discloses that the initial formation of GaN on an AlN layer showed 3D character due to the lattice mismatch between GaN and AlN (Page 826, left-hand column, penultimate paragraph).

D3 makes a similar observation for GaN grown on Si using an AlN buffer layer and mentions cracking of the GaN layer (paragraph [12], right-hand column). Contrary to the arguments of the appellant, the skilled person would thus have considered modifying the structure disclosed in D2 taking into account the teaching of D3.

To solve the problem of 3D-growth and cracking of the GaN epi-layer, D3 proposes to place an amorphous strain-absorbing layer at the interface between the Si substrate and the GaN layer (see paragraph [17]). No AlN layer is placed directly on the Si substrate according to this solution.

Thus, the skilled person, starting from D2 and being confronted with the problem of further enhancing the thickness and quality of the GaN layer, would have consulted D3. Thereby, they would have been led to replace the AlN buffer layer at the Si/GaN interface of D2 by the amorphous strain-absorbing layer of D3.

4.4 Inventive step

It follows from the above that the skilled person, starting from D2 and using their common general knowledge as well as the teaching of D3, would have arrived at the subject-matter of claim 1 of the second auxiliary request without the exercise of an inventive step according to Article 56 EPC 1973.

5. The subject-matter of the independent semiconductor structure claims of all requests lacks an inventive step under Article 56 EPC 1973. Consequently, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated