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Datasheet for the decision of 3 May 2022

Case Number: T 0543/17 - 3.4.03

Application Number: 06803439.6

Publication Number: 1935007

IPC: H01L21/04, H01L21/304, H01L21/306

Language of the proceedings: EN

Title of invention:
METHODS OF PROCESSING SEMICONDUCTOR WAFERS HAVING SILICON CARBIDE POWER DEVICES THEREON

Applicant:
Cree, Inc.

Relevant legal provisions:
EPC Art. 52(1), 123(2)
EPC 1973 Art. 56, 84

Keyword:
Amendments - added subject-matter (no)
Inventive step - (yes)
Claims - clarity and support in the description (yes)

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Case Number: T 0543/17 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 3 May 2022

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Boult Wade Tennant LLP Salisbury Square House 8 Salisbury Square London EC4Y 8AP (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 3 August 2016 refusing European patent application No. 06803439.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	T. Häusser
Members:	M. Ley
	C. Heath

Summary of Facts and Submissions

I. The appeal lies from the decision of the examining division to refuse European patent application No. 06 803 439 pursuant to Article 97(2) EPC.

II. The examining division decided that the subject-matter of claim 1 then on file did not involve an inventive step (Article 56 EPC 1973).

The decision cited the following documents:

D1 WO 01/86727 A2
D2 XP 012026901
D3 US 2004/147120 A1
D4 US 5 851 664 A
D5 WO 2005/048363 A2

III. The appellant requests that the contested decision be set aside and a European patent be granted on the basis of the following documents:

Claims:
No. 1 to 11 filed with letter dated 14 April 2022;

Description:
Pages 1 to 3, 6 to 8, 16 and 17 filed with the letter dated 9 September 2021, pages 5, 9 to 12, 14 and 15 filed with the letter dated 30 December 2021 and pages 4 and 13 filed with letter dated 14 April 2022;

Drawings:
Sheets 1/7 to 7/7 as published.

IV. Claim 1 has the following wording (labelling **(a)** to **(f)** added by the Board):

A method of forming a silicon carbide semiconductor device (110), comprising:
(a) *forming a silicon carbide epitaxial layer (140) on a surface of a silicon carbide substrate (100), the epitaxial layer having a thickness greater than 3 µm;*
(b) *forming a semiconductor device at a first surface of the epitaxial layer (140) opposite the silicon carbide substrate (100);*
(c) *connecting a carrier substrate (105) to the first surface of the epitaxial layer (140);*
(d) *removing the silicon carbide substrate (100) to expose a second surface of the epitaxial layer (140) opposite the first surface while the carrier substrate (105) is providing mechanical support to the epitaxial layer (140);*
(e) *forming a metal layer on the second surface of the epitaxial layer (140); and*
(f) *locally annealing the metal layer to form an ohmic contact (107) on the second surface of the epitaxial layer (140), wherein locally annealing the metal layer comprises locally heating the metal layer to a temperature that is sufficient to cause the metal layer to form the ohmic contact (107) on the second surface of the epitaxial layer (140) but that is lower than a temperature at which the carrier substrate (105) will detach from the epitaxial layer (140).*

Reasons for the Decision

1. The appeal is admissible

2. The invention concerns a method of manufacturing a silicon carbide semiconductor device using a silicon carbide substrate. The application as originally filed describes two main embodiments.

In the first main embodiment, the method has a step of thinning the silicon carbide substrate from a first to a second thickness and forming an ohmic contact on the thinned silicon carbide substrate. Prior to the thinning, a carrier substrate is mounted. Methods according to the first main embodiment are shown in Figures 1A to 1F for the semiconductor device directly formed at a surface of the silicon carbide substrate and in Figures 3A to 3J for the semiconductor device formed at the surface of an epitaxial layer grown on the silicon carbide substrate.

In the second main embodiment, the method has a step of completely removing the silicon carbide substrate and forming an ohmic contact on an exposed second surface of a silicon carbide epitaxial layer, the semiconductor device being at the opposite first surface, see Figures 2A to 2D.

Claim 1 according to the sole request is directed to the second main embodiment.

3. Amendments - Article 123(2) EPC

The Board is satisfied that the set of claims 1 to 11 meets the requirements of Article 123(2) EPC for the following reasons:

3.1 Claim 1 relates to the embodiment shown in figures 2A to 2D, original claims 21 to 26 and paragraphs [0015] to [0018] and [0050] to [0054] of the original description. In particular, claim 1 is based on original claims 21 and 26 as well as paragraphs [0015], [0018], [0036] and [0051] as originally filed.

3.2 By specifying that it is the carrier substrate that provides mechanical support "to the epitaxial layer" in step (d), the added subject-matter objection of section 4.2 of the Board's communication pursuant to Rule 100(2) EPC dated 29 April 2021 is overcome.

The re-introduction of the term "locally" in feature (f) overcomes the added subject-matter objection of section 4.1 of said communication.

3.3 The basis for the dependent claims is the following:

claims 2 and 3: paragraph [0054], Figure 2D
claims 4 to 7: original claims 22 to 25
claim 8: paragraph [0053]
claim 9: paragraph [0037]
claim 10: paragraphs [0009], [0022], [0048], [0062]
claim 11: paragraphs [0013], [0063], original claim 18

In particular, the Board accepts that paragraph [0053] provides a basis for the subject-matter of claim 8, i.e. for locally heating the metal layer comprising laser annealing the deposited metal layer to form an

ohmic contact on an epitaxial layer. The first sentence of paragraph [0053] makes it clear that laser annealing in general can be used in the case of a complete removal of the silicon carbide substrate and the formation of the ohmic contact on the second exposed surface of the epitaxial layer.

The Board also accepts that paragraph [0037] discloses materials of the epitaxial layer 140 of the embodiment of figures 2A to 2D. From the wording "silicon carbide semiconductor device", the skilled person would understand that the epitaxial layer 140 is composed of silicon carbide.

4. Clarity - Article 84 EPC 1973

4.1 The Board notes that the term "locally" had been removed in claim 1 filed on 12 July 2016 after a telephone conversation on 8 July 2016 with the primary examiner, during which an objection under Article 84 EPC has been discussed (see appellant's letter dated 12 July 2016, first page, second paragraph and the impugned decision, Facts and Submissions, point 9). Unfortunately, the Board was not able to find any minutes of this telephone conversation in the electronic file so that it can only speculate about the nature of the alleged lack of clarity.

4.2 The Board notes that an objection under Article 84 EPC 1973 was raised by the examining division against the term "locally annealing", see point 2 of the communication pursuant to Article 94(3) EPC dated 12 August 2010. A similar objection had already been raised in the International Preliminary Report on Patentability under item VIII. After the communication of August 2010, the term "locally" had been removed

from the claims and has been re-introduced only in claim 1 filed on 14 June 2016.

4.3 The Board takes it that the objection under Article 84 EPC 1973 raised during the telephone conversation probably corresponded to the one raised in the communication dated 12 August 2010.

However, the Board does not agree with this objection. The skilled person reading the application and using his common general knowledge understands what is meant by "locally annealing" or "locally heating" a metal layer to form an ohmic contact. The term "locally" implies that the metal layer/epitaxial layer interface is heated without heating e.g. the first surface of the epitaxial layer, see also paragraph [0060] of the description of the application: "Localized annealing may be employed to anneal the ohmic contact 255 on the backside of the thinned wafer 210' without substantially heating the front side of the thinned wafer and the associated device structures". The skilled person would know how to distinguish the claimed local annealing from other annealing processes. For example, it would understand that heating the entire device (including the carrier substrate, the epitaxial layer and the metal layer) in an oven is excluded by the wording of claim 1, because the entire device would then be subjected to the same temperature. The application gives two examples for local annealing (i.e. laser annealing and electron beam annealing) and refers to prior art using localized annealing, see paragraph [0045] of the description. In other words, the skilled person understands the technical meaning of the expression "locally annealing".

The requirements of Article 84 EPC 1973 as to clarity of the claims are therefore fulfilled.

5. Inventive step - Article 56 EPC 1973

5.1 Prior art cited by the examining division

Document D1 discloses a method for fabricating SiC MESFETs, which is similar to the first main embodiment of the application as originally filed. D1 discusses forming epitaxial layers on a silicon carbide substrate, and forming a semiconductor device within the epitaxial layers. The substrate is then partially mechanically thinned using processes such as grinding or lapping (as described on page 16, lines 28 to 30). The thinning process exposes a back surface of the substrate, opposite the surface on which the epitaxial layers are formed. A metal layer is formed on the exposed back surface of the thinned substrate and annealed to form an ohmic contact. The thinned substrate forms an integral part of the final device (see Figure 6I of D1).

D2 describes doping of 6H-SiC by selective diffusion. The SiC device consists of an n^+-type SiC substrate with a 10 µm thick n-doped SiC epitaxial layer. A p-n diode is fabricated by forming a local p-type emitter region on the n-type epitaxial layer, see Figure 1. Metal layers are deposited as contacts on the p-type region at the underside of the substrate. The devices are annealed in a vacuum in order for the metal layers to form ohmic contacts. As such, D2 does not disclose a method of forming a device in which the substrate is thinned or completely removed.

D3 describes a process for the back-surface grinding of wafers. The process uses a film 3 having a support layer 5 and an adhesion layer 4, the adhesion layer used to attach the support layer to a front surface of the device. The adhesion layer can match the contours and shape at the surface of the device, whereas the rear side of the support layer runs plane-parallel to the wafer surface (see Figure 1). A first photochemical partial polymerization causes the adhesion layer to increase the adhesion to the front surface of the wafer, see paragraph [0023]. The grinding of the back surface of the wafer may then take place. Then, a second partial polymerization results in a decrease in the adhesion of the support layer to the wafer surface, in order to allow the film to be removed, see paragraph [0025].

D4 describes semiconductor wafer thinning processing using adhesives and tapes. The tape described includes a permanent backing and a layer of non-pressure sensitive adhesive. The tape can be used as a support during grinding or dicing of a semiconductor wafer.

D5 describes a method of processing the back-side of a semiconductor wafer for the fabrication of light emitting diodes; the method including thinning (e.g. by grinding or polishing) a silicon carbide substrate in order to change the forward operating voltage of the light emitting device. In relation to Figures 1 to 7, D5 describes forming devices 110 (e.g. GaN-based epitaxial layers) on a silicon carbide substrate 100, and connecting a wafer carrier 105 to the substrate so that the back side of the substrate 100 can be accessed. The wafer carrier 105 is attached via an adhesive layer 120. The back side of the substrate is then processed to form a thinned wafer 100', see e.g.

Figure 3. The silicon carbide substrate may be thinned using an in-feed or creep-feed grinder. The wafer carrier 105 can then be removed, in order to perform subsequent processing of the devices. However, in every described embodiment the thinned substrate forms the basis for the final devices.

5.2 Both the examining division and the appellant used document D1 as the closest prior art. The Board sees no reasons to deviate from this choice.

In the wording of claim 1, D1 discloses a method of forming a silicon carbide semiconductor device (Figures 5 and 6A to 6I), comprising:
forming a silicon carbide epitaxial layer (13, 14; page 19, line 31; page 21, lines 1 and 2) on a surface of a silicon carbide substrate (10; page 19, line 32), ~~the epitaxial layer having a thickness greater than 3 microns~~;
forming a semiconductor device at a first surface of the epitaxial layer (Figures 6C to 6G) opposite the silicon carbide substrate (10);
~~connecting a carrier substrate to the first surface of the epitaxial layer~~;
~~removing~~ thinning (Figures 6G, 6H; page 16, lines 28 to 30; page 22, lines 3 to 5) the silicon carbide substrate (10) to expose a second surface of the thinned silicon carbide substrate (10') ~~of the epitaxial layer opposite the first surface while the carrier substrate is providing mechanical support to the epitaxial layer~~;
forming a metal layer (32; figure 6I) on the second surface of the thinned silicon carbide substrate ~~of the epitaxial layer~~; and
~~locally~~ annealing the metal layer to form an ohmic contact (32; Figures 5 and 6I; page 16, lines 26 to 33)

on the second surface of the thinned silicon carbide substrate ~~of the epitaxial layer~~, wherein ~~locally~~ annealing the metal layer comprises heating the metal layer to a temperature that is sufficient to cause the metal layer to form the ohmic contact on the second surface of the thinned silicon carbide substrate (page 22, lines 15 to 17) ~~of the epitaxial layer but that is lower than a temperature at which the carrier substrate will detach from the epitaxial layer~~.

In view of the above, the method according to claim 1 differs from the one of D1 by the following distinguishing features :

(i) the epitaxial layer has a thickness greater than 3 µm
(ii) a carrier substrate is connected to the first surface of the epitaxial layer,
(iii) the silicon carbide substrate is removed to expose a second surface of the epitaxial layer opposite the first surface while the carrier substrate is providing mechanical support to the epitaxial layer
(iv) the metal layer is formed on the second surface of the epitaxial layer
(v) the ohmic contact is formed by locally heating the metal layer to a temperature that is sufficient to cause the metal layer to form the ohmic contact on the second surface of the epitaxial layer but that is lower than a temperature at which the carrier substrate will detach from the epitaxial layer.

These five distinguishing features substantively correspond to those identified by the appellant, see the statement setting out the grounds of appeal, page 2.

5.3 The appellant argued that the objective problem solved by these features was to provide a more reliable method for fabricating a silicon carbide power device. It referred to paragraphs [0065] and [0066] of the description of the application to show that the devices according to the present invention resulted in a reduced device area for a given on-state resistance, which could lead to a higher device yield and/or lower costs.

The Board is not convinced by these arguments, because the application as originally filed does not provide any indication that the method known from D1 would be less reliable than the claimed one. The advantages mentioned in paragraphs [0065] and [0066], e.g. reduced on-state resistance, are obtained for power devices made by a method according to claim 1 (i.e. with removal of the SiC substrate) or a method according to D1 (i.e. with a thinning of the SiC substrate).

5.4 The Board identified two partial objective technical problems related to feature (i) and features (ii) to (v), respectively.

5.4.1 Regarding (i), there is no disclosure in the application as originally filed that the epitaxial layer contributes to the mechanical stability due to its thickness. The objective technical problem is to select a suitable dimensions for epitaxial layer 13, 14 in D1, which is composed of first and second epitaxial sub-layers 13 and 14.

The thickness of the first epitaxial layer is 0.5 to 2 µm according to page 17, lines 8 to 15 of D1. The thickness of the second epitaxial layer 14 is not explicitly disclosed in D1, but it is stated that it is

selected according to the desired pinch-off voltage, see D1, page 18, lines 1 to 8. It would be obvious for the skilled person to select a thickness of epitaxial layer 14 of greater than 1 µm so that a total thickness of the epitaxial layer 13, 14 of greater than 3 µm would be achieved.

5.4.2 Regarding features (ii) to (v), the objective technical problem associated thereto is to improve the thermal performance of the device known from D1.

The Board agrees with the examining division that it might be obvious for the skilled person to connect a carrier substrate providing a mechanical support, when thinning silicon carbide substrate 10 of D1 as shown in figures 6G and 6H. As pointed out by the examining division, this aspect is also known from D5, see Figures 1 to 3, wherein a support substrate 105 is used when thinning a semiconductor wafer 100. In other words, distinguishing feature (ii) alone might be obvious for the skilled person.

Page 17, lines 1 to 2 of D1 states that the thermal performance of the device known from D1 is improved by thinning the wafers before metallization, as shown for the silicon carbide substrate 10 in Figures 6G and 6H. The skilled person wishing to solve the objective technical problem would hence have a motivation to further reduce the thickness of substrate 10. It would, however, not get an incentive to completely remove substrate 10 and provide metallisation 32 directly on an exposed backside of epitaxial layer 32. Neither one of the prior art documents D2 to D5 at hand - see section 5.1 above - nor document D1 itself disclose or suggest that the silicon carbide substrate 10 could be

completely removed to expose a second surface of the epitaxial layers 13, 14 opposite the first surface.

Even if the skilled person would know from its common general knowledge that a silicon carbide substrate could be completely removed from an epitaxial layer, it would not apply this knowledge to the method of D1. In D1, the epitaxial layers 13 and 14 as well as the substrate 10/10' are etched to form isolation mesas, on which a passivation layer 60 is formed, see figure 6B and page 20, line 33 to page 21, line 3. In other words, after the step shown in figure 6B, the plurality of mesas are in mechanical contact through substrate 10/10'. In figure 6I, metallization layer 32 is formed on the (thinned) substrate 10' and functions as conducting plane (page 15, line 16 to 19; page 22, lines 5 and 6) to improve the device packaging by permitting easier attachment of the device to a circuit board (page 16, lines 26 to 33). The skilled person understands from D1 that metallization layer 32 is a conducting plane common to a plurality of mesas, each forming one MESFET, if not to all. Hence, the skilled person understands from D1 that, in order to provide the function of metallization layer 32 as a common conducting plane, thinned substrate 10' supporting metallization layer 32 cannot be completely removed.

Moreover, in D1, the thinned substrate 10' has a thickness of 25 to 100 µm (page 16, line 29) and layer 13 is 0.5 to 2 µm thick (page 17, lines 8 to 15). As mentioned already above, the thickness of layer 14 is not disclosed. In order to completely remove substrate 10 and at the same time maintain the mechanical stability of the device, the skilled person would have to grow layers 13 and 14 thicker than 25 µm and thus make the transistors much larger. Furthermore, it would

have to form the mesa structure in layers 13 and 14 alone and find other ways to laterally isolate the transistor shown in drawing 6I. The Board is of the opinion that the skilled person would not consider this arrangement.

For the Board, feature (iii) is therefore not obvious in view of the prior art at hand and the common general knowledge of the skilled person.

Regarding features (iv) and (v), the Board agrees with the examining division that a skilled person using his common general knowledge would perform the heating of the metal layer at a temperature sufficiently high to achieve the desired ohmic contact and sufficiently low in a way not to damage the device, regardless whether the ohmic contact is formed on the silicon carbide substrate as in D1 or on the epitaxial layer. In the example of D1, it would wish to avoid a pre-mature detaching of the epitaxial layer from a carrier substrate. Locally annealing a metal layer e.g. by a laser beam to form an ohmic contact is also known in the art (see paragraph [0045] of the description of the application). It would be obvious to use this technique in the method of D1.

However, as the Board considers that feature (iii) is not rendered obvious, the skilled person would not provide the metal layer on an exposed second surface of the epitaxial layer in D1 in order to form the ohmic contact (feature (iv)), either.

5.5 The examining division argued that "it might effectively be difficult to determine whether the substrate is completely removed or only thinned" as "an epitaxial silicon carbide layer deposited on a

crystalline silicon substrate is not necessarily distinguishable from the latter", see the contested decision, point 3 of the Reasons.

The appellant argued that an epitaxial layer was always distinguishable from the substrate due to its "advantageous properties" like higher purity, fewer defects or improved electron mobility.

The argumentation given by the examining division cannot be followed by the Board. In case of an homoepitaxial layer, i.e. an epitaxial layer made of SiC on an SiC substrate, a skilled person would be able to determine if a substrate has been removed or is merely thinned. For example, in case of a 10 µm thick SiC epi-layer grown on a 200 µm thick SiC substrate, if after a grinding step, a thickness t of 10 µm (or less) of SiC is left, the substrate has been completely removed. If a thickness t larger than 10 µm of SiC is left, then the substrate has been merely thinned, namely by an amount of 210 µm minus t.

5.6 In view of the above, the subject-matter of claim 1 is not rendered obvious to the skilled person, neither by document D1 alone nor by the combination of document D1 with any of documents D2 to D5. Hence, the claimed subject-matter involves an inventive step (Article 52(1) EPC and Article 56 EPC 1973).

6. Adaptation of the description

By indicating in the description that the subject-matter shown in figures 1A to 1F and 3A to 3J illustrate methods of processing semiconductor wafers according to examples "providing background information useful to understanding the invention" and by

specifying that the features according to claim 1 are not qualified as optional features in the description, the Board is satisfied that there will remain no inconsistencies between the description and the claims with the result that the claims are supported by the description as required by Article 84 EPC 1973, second sentence.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent in the following version:

Claims:
No. 1 to 11 filed with letter dated 14 April 2022;

Description:
Pages 1 to 3, 6 to 8, 16 and 17 filed with the letter dated 9 September 2021, pages 5, 9 to 12, 14 and 15 filed with the letter dated 30 December 2021 and pages 4 and 13 filed with letter dated 14 April 2022;

Drawings:
Sheets 1/7 to 7/7 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero T. Häusser

Decision electronically authenticated