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Datasheet for the decision of 27 July 2021

Case Number: T 0715/17 - 3.4.03

Application Number: 07809749.0

Publication Number: 2036122

IPC: H01L21/8247, H01L27/115

Language of the proceedings: EN

Title of invention:
MEMORY DEVICES HAVING REDUCED INTERFERENCE BETWEEN FLOATING GATES AND METHODS OF FABRICATING SUCH DEVICES

Applicant:
Micron Technology, Inc.

Headword:

Relevant legal provisions:
RPBA 2020 Art. 13(2)
EPC 1973 Art. 111(1), 54(2)

Keyword:
Novelty - (no)
Amendment after summons - taken into account (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
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Beschwerdekammern

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Case Number: T 0715/17 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 27 July 2021

Appellant: (Applicant)	Micron Technology, Inc. 8000 South Federal Way Boise, ID 83707-0006 (US)
Representative:	Gill Jennings & Every LLP The Broadgate Tower 20 Primrose Street London EC2A 2ES (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 20 October 2016 refusing European patent application No. 07809749.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	A. Böhm-Pélissier
	G. Decker

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division to refuse European patent application No. 07 809 749. The refusal was based on the ground of unallowable amendments (Article 123(2) EPC). In an *obiter dictum* not forming part of the decision, the Examining Division provided reasons as to why the subject-matter of claim 1 was not novel over the disclosure of document D2.

II. The oral proceedings before the board were held by videoconference with the agreement of the Appellant. The Appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the claims according to the Main Request filed with letter dated 25 August 2016, or alternatively, on the basis of the First Auxiliary Request filed during oral proceedings before the Board.

III. Highlighting (additions, ~~deletions~~, **bold**) and labelling in citations are added by the Board.

IV. **Claim 1** of the **Main Request** reads as follows:
(A) A method (128) of fabricating a floating gate memory array (32, 52) comprising:
(B) forming (130) a gate oxide layer (110) on a substrate (108);
(C) forming (132) a floating gate layer (-) on the gate oxide layer (110);
(D) forming (134) an inter-gate dielectric layer (120) directly on the floating gate layer (112);
(E) etching (136) the substrate (108), the gate oxide layer (110), the inter-gate dielectric layer (120) and the floating gate layer to form:

(F) a plurality of pillars (118) in the substrate (108) separated by one or more trenches;
(G) a plurality of the floating gates (112), wherein each of the plurality of floating gates (112) corresponds to one memory cell and is on one of the plurality of pillars; and
(H) a plurality of electrically isolated inter-gate dielectric regions (120A-120C),
(I) wherein each of the plurality of electrically isolated inter-gate dielectric regions (120A-120C) corresponds to one memory cell, is directly on one of the plurality of floating gates,
(J) and is electrically isolated from each other of the plurality of electrically isolated inter-gate dielectric regions (120A-120C) corresponding to other memory cells; and
(K) forming (142) a control gate (122) directly on the plurality of electrically isolated inter-gate dielectric regions (120A-120C);
characterized in that:
(L) the plurality of floating gates (112) and the plurality of electrically isolated inter-gate dielectric regions (120A-120C) are formed in a same processing step (136) before a processing step used to form the control gate (122).

V. Claim 1 of the (**First) Auxiliary Request** reads:
[Features (A) to (K)]
(L1) the plurality of floating gates (112) and the plurality of electrically isolated inter-gate dielectric regions (120A-120C) are formed in a same processing step (136) before ~~a~~ any processing step used to form the control gate (122).

VI. Documents cited in this decision:

D2 = US 2003/151084 A1
D3 = US 2005/067652 A1
D4 = US 2006/060927 A1
D6 = US 2005/003619 A1

VII. The **Appellant argued** essentially as follows:

(a) in D2 the word line cannot be considered to be (part of) the "control gate";

(b) in D2 the control gate layer 58c is not formed in a separate step after forming the floating gate layer and the inter-gate dielectric layer;

(c) the Auxiliary Request should be admitted into the proceedings because it was a reaction to developments during the oral proceedings before the Board and because it overcame the novelty objections.

Reasons for the Decision

1. The appeal is **admissible**.

2. The invention as claimed

2.1 The present invention concerns a NAND flash memory device with Shallow Trench Isolation (STI) for preventing current leakage between adjacent transistors.

2.2 With the ever-decreasing device geometries, the extreme density of the memory devices introduces a number of undesirable inter-component interactions such as capacitive interference between adjacent memory cells. This is of growing concern as the size of the memory

cells decrease. For floating gate memory cells in particular, current leakage between adjacent floating gates is to be reduced. High-k materials are employed to reduce tunneling current and out diffusion from the floating gate and the control gate. However, the high-k material also has the disadvantageous effect of increasing the FG-FG capacitance through the inter-gate dielectric layer (see paragraph [0036] of the application).

2.3 In order to reduce those interferences, the application in suit proposes that all inter-gate dielectric regions (corresponding to one memory cell) are electrically isolated from each other and formed in the same processing step with the floating gates before the control gates are formed.

3. **Main Request**

3.1 Terminology

For assessing the requirements of novelty it was essential to clarify how the skilled person understands the terms "forming" and "processing step".

3.1.1 "Forming"

The Appellant and the Board agreed that a forming step comprises - in the light of the description - at least one step where a layer or a plurality of layers is deposited, structured by etching / patterning or where the form of a structure (e.g. transistor) is finalised. In the application in most cases "forming" is used in the sense of "etching" or "patterning" (e.g. "forming the trenches"). On the other hand, "forming" can be considered equivalent to "depositing" (e.g. paragraph

[0033], "*... a control gate, which may be formed of a single conductive layer*").

Forming a layer may comprise several stages: an initial stage, where a part of the layer is deposited and etched, e.g. in the bit line (column) direction (forming the trenches), and a final stage, where the layer is finalised, e.g. by etching a structure in the word line (row) direction.

3.1.2 Processing step

A "processing step" could comprise:
(a) a deposition step of depositing a single layer or a plurality of layers;
(b) an etching step of etching / patterning a single layer or a plurality of layers;
(c) other steps, such as providing photosensitive material, application of a mask pattern, removing photosensitive material, planarisation, preparation of subsequent depositing or patterning steps etc.

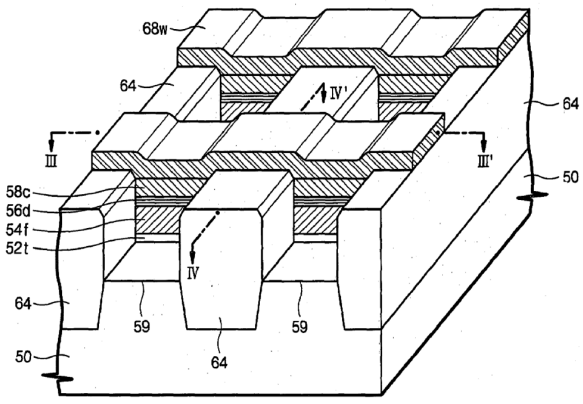
Each sub-step may already be considered a layer forming step or processing step, even if the form of the layer is not finalised in this (sub-)step. On the other hand, etching a plurality of layers in one etching procedure may be considered to be one processing step.

3.2 Novelty

3.2.1 It was undisputed that **D2** discloses **features (A) to (K)**. In particular, D2 discloses an inter-gate dielectric layer 56d isolated from each other inter-gate dielectric layer and etching the floating gate layer 54f together with the inter-gate dielectric layer 56d in one and the same processing step. Etching takes

place twice. First, when the trenches 64 are etched. Second, when the word lines 68w - together with the layers 58c, 56d, 54f and 52t beneath the word line - are etched (paragraph [0035]).

- 68w word line
- 58c control gate electrode
- 56d inter-gate dielectric layer
- 54f floating gate layer
- 52t gate oxide layer
- 50 substrate
- 59 active regions
- 64 trench isolation



D2, Fig. 4

3.2.2 As to **feature (L)** the Appellant argued that the word line 68w in D2 could not be considered to be (part of) a control gate. The word line supplied a plurality of memory stacks, but did not act as a control gate. Therefore, the concept that the control gate was construed as a combination of word line 68w and control gate layer 58c was void and the subject-matter of claim 1 was novel over D2.

3.2.3 The Board however is of the opinion that in D3, D4 and D6 examples are provided where a shared control gate layer / word line - as in the present application - is directly in contact with the inter-gate dielectric layer without an intermediate control gate electrode. In D4 (Fig. 13) the (shared) control gate 7 directly contacts the dielectric layers 6/5 in absence of a control gate electrode. In D6, Fig. 10, word line 10 forms the control gate and is in direct contact with the inter-gate dielectric layer 8d. In these examples a control gate electrode is not used in analogy to the present invention.

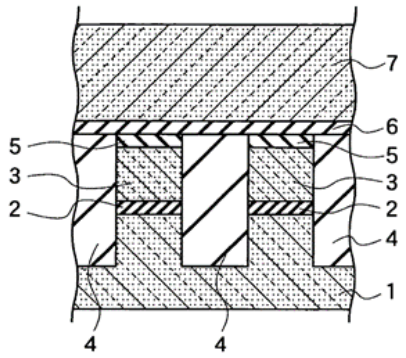


Fig. 13 of D4

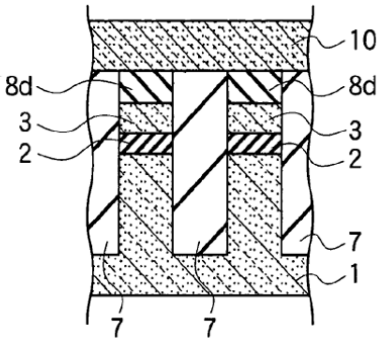


Fig. 10 of D6

3.2.4 D6 discloses alternative embodiments, where a control gate electrode 9 is used in a similar manner as disclosed in D2.

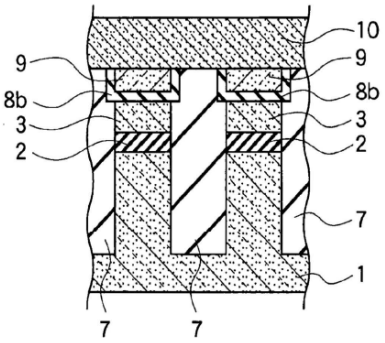


Fig. 6 of D6

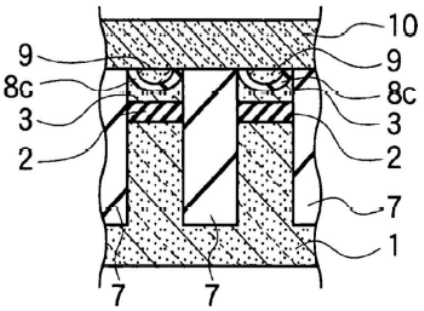


Fig. 8 of D6

3.2.5 Patterning a control gate electrode ("auxiliary conductive layer serving as control gate electrode", D6, paragraph [0046], Figs. 6 and 8) or omitting (Fig. 10 of D6) such an electrode are therefore alternative options. Also in D3 a shared control gate 2 is directly deposited onto the inter-gate dielectric layer 7. Control gate 2 forms a unit of control gate supply (upper part) and control gate electrode (lower part of layer 2).

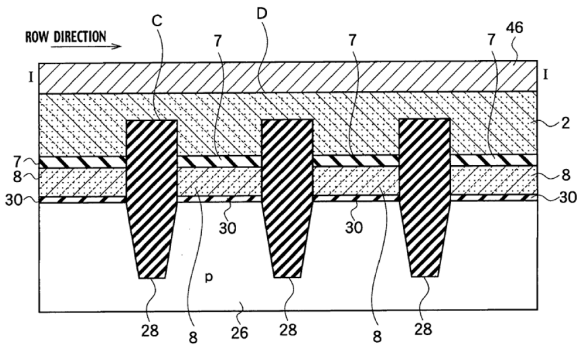


Fig. 18 of D3

3.2.6 The word line (shared control gate layer) in these examples is in direct contact with the inter-gate dielectric layer without any intermediate (control gate electrode) layer and acts both as control gate supply and control gate electrode. Furthermore, in D2 both the control gate electrode 58c and the word line 68w are made of the same conductive material, i.e. poly-silicon (cf. D2, paragraphs [0031] and [0035]) and therefore could be considered to be a control gate unit. Consequently, control gate electrode 58c and word line 68w can be considered to be the "control gate" mentioned in feature (L). Word line layer 68w (part of the "control gate") is formed (deposited, etched and finalised) after forming (depositing and etching) floating gate layer 54f and inter-gate dielectric layer 56d.

3.2.7 The Appellant further argued that D2 disclosed in paragraph [0033] that *"the hard mask layer 60, the control gate layer 58, the dielectric layer 56, the floating gate layer 54, the oxide layer 52, and the semiconductor substrate 50 are successively patterned to form trenches 61 in the semiconductor substrate 50 to define a plurality of active regions 59" (emphasis added).* D2 therefore appeared to describe *successively* patterning a dielectric layer and a floating gate layer in two separate processing steps. Hence, D2 did not

teach or suggest etching an inter-gate dielectric layer and a floating gate layer in the same processing step as recited in independent claim 1.

3.2.8 The Board however notes that "processing step" has a broad meaning and could comprise several sub-steps (see section 3.1.2 above). In view of the structure of active region 59 in Fig. 4 of D2 it would make no sense that each layer 52t to 58c is etched or patterned separately. The expression "*successively*" has to be understood that in one and the same processing step the layers are successively etched in the depth direction, e.g. "drilled" down by dry etching. In D2 layers 54f and 56d are therefore considered to be formed in the same etching step.

3.2.9 **Floating gate layer 54f and inter-gate dielectric layer 56d** are formed in three separate "same processing steps", wherein "forming" comprises depositing or etching (see Fig. 4 of D2):

(a) depositing layers 54f and 56d (together with layers 52t and 58c);

(b) etching layers 54f and 56d when etching trenches 64, i.e. successively etching layers 58c, 56d, 54f and 52t;

(c) etching layers 56d and 54f when successively etching word line layer 68w, layers 58c, 56d, 54f and 52t.

3.2.10 The **control gate** is also formed in three separate "forming processing steps":

(i) depositing layer 58c onto layer 56d;

(ii) etching gate electrode layer 58c when etching trenches 64, i.e. successively etching layers 58c, 56d, 54f and 52t;

(iii) forming the word lines 68w, i.e. successively etching word line layer 68w, control gate layer 58c, layers 56d, 54f and 52t.

3.2.11 Forming step (a) takes place before control gate forming steps (ii) and (iii). Forming step (b) takes place before control gate forming step (iii).

3.2.12 Therefore, D2 discloses that the plurality of floating gates (54f) and the plurality of electrically isolated inter-gate dielectric regions (56d) are formed in a same processing step [(a) or (b)] before **a** processing step used to form the control gate (58c) [steps (a) and (b) take place before step (iii), step (a) takes place before step (ii)]. Consequently, D2 discloses feature (L) and the subject-matter of claim 1 of the Main Request is not novel over document D2.

4. **Auxiliary Request - Admission under Article 13(2) RPBA 2020**

4.1 In order to overcome the novelty objection discussed above, the Appellant filed an Auxiliary Request during oral proceedings. The request was intended to delimit the forming process of the present application from the process described in D2.

4.2 According to Article 13(2) RPBA 2020, any amendment to a party's appeal case made after notification of a summons to oral proceedings should, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned.

When exercising its discretion under Article 13(2) RPBA 2020, the Board may also rely on criteria as set out in Article 13(1) RPBA 2020 (see section VI of document CA/3/19, explanatory remarks on Article 13(2) RPBA 2020, page 43 first full paragraph). One criterion under said provision is whether the party has demonstrated that any amendment to a patent application, *prima facie*, overcomes the issues raised by the Board and does not give rise to new objections.

4.3 The Appellant argued that in the present invention the control gate 122 was formed in a completely separate process after forming both floating gate layer 112 and the inter-gate dielectric layer 120A-120C in a same processing step. No combination of these steps took place in the present invention in contrast to D2, where the control gate 58c was etched in the same processing step as the floating gate 54f and the inter-gate dielectric layer 56d. D2 was accidentally novelty destroying for the Main Request, as the process of D2 was completely different with respect to the present application. Therefore, feature (L1) was amended accordingly in order to further distinguish the claim from the disclosure of D2.

4.4 The Board is of the opinion that the amendment is *prima facie* contradicting the original teaching of the present application. In the present invention the second etching step is performed in analogy to step (iii) in D2 when the word lines are formed. The corresponding structure is shown in Fig. 11 of the present application. Fig. 11 shows that layers 122 (word line), inter-gate dielectric regions (120A-120C), floating gate (112) and gate oxide layer (110) were patterned in one and the same processing step. In the alternative embodiment described in Fig. 12 and in

paragraph [0047] only the step of forming the inter-gate dielectric layer 120A-120C is replaced by a process without sacrificial silicon nitrite layer. The ultimate forming step of patterning the word line is the same as in the first embodiment. The result of this patterning step is shown in Fig. 11. From the description of Fig 11 (paragraph [0046]: "*That is, in the view shown in FIG. 11, the word lines WL extend into the page*") and Fig. 11 itself the skilled person would deduce that layer 122 is a shared common control gate (cf. paragraph [0033]) or word line. The skilled person understands from Fig. 11 in the context of the previous figures and the description that layers 122, 120A-120C, 112 and 110 are successively etched, i.e. drilled down by means of dry etching until the substrate 108 is reached. Control gate layer 122 is necessarily removed before removing the inter-gate dielectric layer 120A-120C and the floating gate layer 112. This however is in contradiction to amended feature (L1). Therefore, the amendment in feature (L1) is in contradiction to the teaching of Fig. 11 and cannot be considered to comply with Article 123(2) EPC.

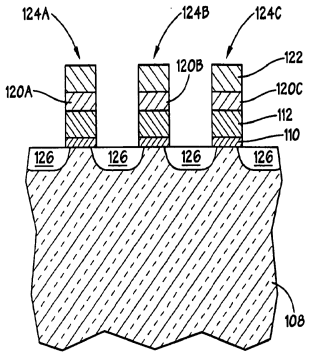


Fig. 11 of the application

4.5 Furthermore, the feature "before any processing step used to form the control gate" excludes any other step related to forming the control gate electrode prior to the ultimate step of forming layers 112 and 120A-120C.

However, the Board could not find a direct and unambiguous disclosure in the application as originally filed that **any** processing step (including preparation of deposition, planarisation, etching or preparation of any processing devices linked to any processing step of forming the control gate) - taking place before forming the floating gate and inter-gate dielectric layer - is excluded. Such a "strong" feature would need an explicit basis in the application as originally filed, in particular if this feature is in contradiction to the teachings of Fig. 11 (see previous section).

4.6 Consequently, feature (L1) does *prima facie* not comply with the requirements of Article 123(2) EPC.

4.7 Furthermore, the Board has doubts that the subject-matter of claim 1 is inventive. The Board agrees with the Appellant that the process of D2 is different in that in the present invention a control gate electrode (58c in D2) is not used and the control gate contact is made directly between the control gate (122 in the present invention) and the inter-gate dielectric layer (120A-120C in the present invention). The present application however is silent about any effect related to this distinguishing feature (which may have the advantage of simplifying the forming process and avoiding any oxidation or contamination between the control gate electrode and the control gate layer). Omitting the control gate electrode however is a normal option when forming a "GC stack". This is e.g. taught in D4 (Fig. 13) and in D6, Fig. 10 (see sections 3.2.3 to 3.2.6 above). Patterning a control gate electrode or omitting such an electrode are hence alternative options (see above). Furthermore, D3 teaches in paragraph [0049] that "*the floating gates 8 and the control gates 2 of the GC stacked structure are formed*

separately". In D2 both the control gate electrode and the word line are made of the same material. The Board is therefore of the opinion that the skilled person would apply the teachings of any of D3, D4 and D6 to the teaching of D2 and omit a separate gate electrode layer 58c (or form the gate electrode and the word line in one processing step) in order to achieve the corresponding advantages. Adapting the process of D2 accordingly would result in a process according to claim 1.

4.8 Therefore, the Board, exercising its discretion under Article 13(2) and (1) RPBA 2020, does not admit the Auxiliary Request into the proceedings.

5. In **summary**, since the Auxiliary Request is not admitted into the proceedings because it does not *prima facie* comply with the requirements of the EPC, and the subject-matter claimed according to the Main Request is not novel over D2 within the meaning of Articles 52(1) EPC and 54(2) EPC 1973, the Examining Division's decision refusing the application is confirmed. Consequently the appeal has to be dismissed (Articles 97(2) EPC and 111(1) EPC 1973).

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated