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Datasheet for the decision of 18 February 2021

Case Number: T 0967/17 - 3.5.03

Application Number: 09252891.8

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Language of the proceedings: EN

Title of invention:
Current controlled shunt regulator

Applicant:
Hamilton Sundstrand Corporation

Headword:
FET shunt regulator/HAMILTON

Relevant legal provisions:
EPC Art. 56, 84, 123(2)
EPC R. 100(2)
RPBA 2020 Art. 13(1)

Keyword:
Decision in written proceedings - (yes)
Admittance of main request filed in response to a communication under R. 100(2) EPC - (no): not clearly allowable
Added subject-matter - auxiliary request (no, after amendments)
Clarity - auxiliary request (yes, after amendments)
Inventive step - auxiliary request (yes, after amendments)

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Case Number: T 0967/17 - 3.5.03

D E C I S I O N
of Technical Board of Appeal 3.5.03
of 18 February 2021

Appellant: (Applicant)	Hamilton Sundstrand Corporation One Hamilton Road Windsor Locks, CT 06096-1010 (US)
Representative:	Dehns St. Bride's House 10 Salisbury Square London EC4Y 8JD (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 7 October 2016 refusing European patent application No. 09252891.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	K. Bengi-Akyürek
Members:	K. Peirs
	N. Obrovski

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing the present European patent application for lack of inventive step (Article 56 EPC).

II. In the impugned decision, the following prior-art documents were referred to in connection with the objection of lack of inventive step:

D1: GB 2 301 240 A;

D2: M. REDDIG: "Optimization of the input and output stages in high efficiency power supplies", IEEE International Conference on INDUSTRIAL TECHNOLOGY 2003, vol. 2, pp. 1190-1195, 10 December 2003.

III. With the statement of grounds of appeal, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claim request underlying the decision under appeal.

IV. In response to a communication from the board pursuant to Rule 100(2) EPC, the appellant filed an amended set of claims along with amended pages of the underlying description as per a **main request** and a **first auxiliary request**.

It was added that "[i]n the event that neither the Main Request nor the First Auxiliary Request are allowable, we maintain our request for Oral Proceedings".

V. Claim 1 of the **main request** reads as follows:

"An electrical system comprising a number of electrical phases and including a field effect transistor FET shunt regulator, the FET shunt regulator comprising; [sic]

a rectifier (120);

a controller (122); and

a plurality of FET shunts (110) equal to the number of electrical phases of the electrical system (100);

wherein each of said FET shunts corresponds to a phase of the electrical system and is connected in such a way as to allow power to travel unimpeded between said corresponding phase of said electrical system and said rectifier when said FET shunt is off and redirect current from said corresponding phase of said electrical system to neutral when said FET shunt is on;

characterised in that:

the FET shunt regulator further comprises a plurality of comparators (124), each of which has a comparator input connected to a corresponding phase of said electrical system;

each of said comparators is arranged to determine if a phase voltage of the corresponding phase is positive or negative, and is arranged to output a corresponding comparator control signal indicating that a corresponding FET shunt of the plurality of FET shunts should be turned on when the phase voltage is negative, and to not output the corresponding comparator control signal when the phase voltage of the corresponding phase is positive;

wherein said controller is arranged to output a controller control signal indicating whether the FET shunts should be turned on;

wherein the FET shunt regulator further

comprises a plurality of logical OR gates (118) each corresponding to a FET shunt of the plurality of FET shunts, wherein each OR gate comprises a first input and a second input and is arranged to receive and combine the corresponding comparator control signal as the first input and the controller control signal as the second input, and to output a FET shunt control signal to a gate of the corresponding FET shunt;

wherein each of said FET shunts (110) is arranged to receive the FET shunt control signal from a corresponding logical OR gate of the plurality of logical OR gates (118);

wherein said controller is arranged to output the controller control signal identically to each FET shunt so that all FET shunts are activated simultaneously whenever the controller indicates that the FET shunts should be turned on,

and wherein each of said logical OR gates is arranged to output the FET shunt control signal to turn said corresponding FET shunt on whenever either the corresponding comparator control signal as the first input or the controller control signal as the second input indicate that the corresponding FET shunt should be turned on."

VI. Claim 1 of the **first auxiliary request** reads as follows (underlining added by the board to reflect the changes with respect to claim 1 of the main request):

"An electrical power generating system comprising a multiphase permanent magnet alternator (100) and a current controlled shunt regulator, the current controlled shunt regulator comprising;[sic]

a rectifier (120);

a controller (122); and

a plurality of field effect transistor FET shunts (110) equal to the number of electrical phases of the permanent magnet alternator (100);

wherein each of said FET shunts corresponds to a phase of the permanent magnet alternator and is connected in such a way as to allow power to travel unimpeded between said corresponding phase of said permanent magnet alternator and said rectifier when said FET shunt is off and redirect current from said corresponding phase of said permanent magnet alternator to neutral when said FET shunt is on; characterised in that:

the current controlled shunt regulator further comprises a plurality of comparators (124), each of which has a comparator input connected to a corresponding phase of said permanent magnet alternator;

each of said comparators is arranged to determine if a phase voltage of the corresponding phase is positive or negative, and is arranged to output a corresponding comparator control signal indicating that a corresponding FET shunt of the plurality of FET shunts should be turned on when the phase voltage is negative, and to not output the corresponding comparator control signal when the phase voltage of the corresponding phase is positive;

wherein said controller is arranged to output a pulse width modulated controller control signal indicating whether the FET shunts should be turned on;

wherein the current controlled shunt regulator further comprises a plurality of logical OR gates (118) each corresponding to a FET shunt of the plurality of FET shunts, wherein each OR gate

comprises a first input and a second input and is arranged to receive and combine the corresponding comparator control signal as the first input and the pulse width modulated controller control signal as the second input, and to output a FET shunt control signal to a gate of the corresponding FET shunt;

wherein each of said FET shunts (110) is arranged to receive the FET shunt control signal from a corresponding logical OR gate of the plurality of logical OR gates (118);

wherein said controller is arranged to output the pulse width modulated controller control signal identically to each FET shunt so that all FET shunts are activated simultaneously whenever the controller indicates that the FET shunts should be turned on,

and wherein each of said logical OR gates is arranged to output the FET shunt control signal to turn said corresponding FET shunt on whenever either the corresponding comparator control signal as the first input or the pulse width modulated controller control signal as the second input indicate that the corresponding FET shunt should be turned on."

Reasons for the Decision

1. *Decision in written proceedings*

The appellant requested oral proceedings in the event that neither the main request nor the first auxiliary request is allowable (cf. point IV above). In view of the allowability of the first auxiliary request, the

decision could be taken in written proceedings (Article 116(1) EPC).

2. *The present application*

2.1 The invention relates to power rectification with a field-effect transistor (FET) shunt regulator. The invention's power-rectification circuit relies on a FET shunt regulator and, like all circuits, necessarily consists of a closed loop between the power source and the ground (see Figure 1 below). When the FET is in the open state, power rectification by conventional means may require to achieve this closed loop by a forced "body-drain" connection within the transistor. Such a forced "body-drain" connection causes considerable power losses and a reduced lifetime of the transducer.

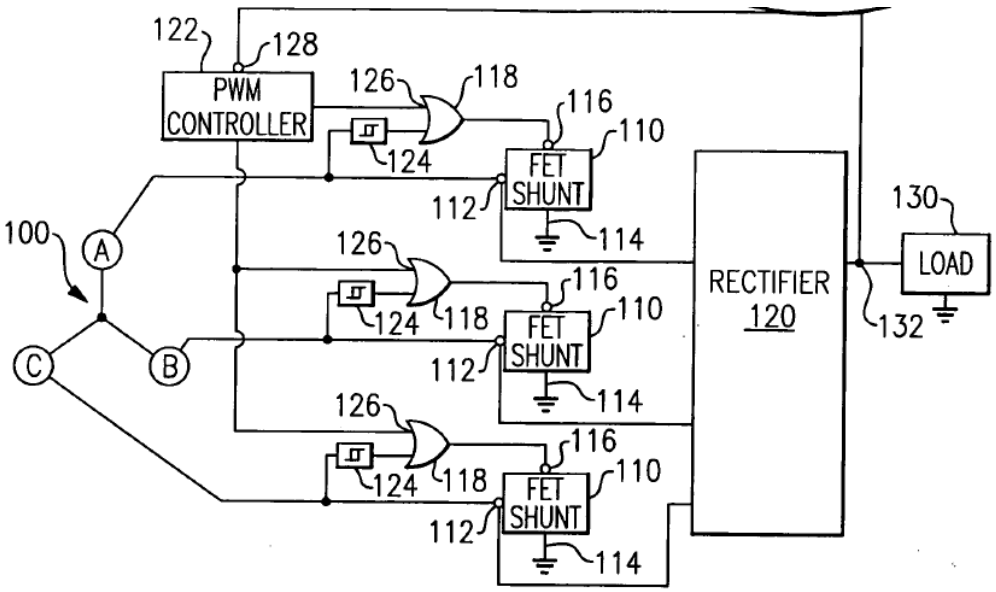

FIG.1

2.2 The invention overcomes this by using a logical "OR" gate 118 for each FET shunt 110 comprised by the FET shunt regulator. This "OR" gate ensures that the FET shunt is "on" (i.e. is conducting) in two situations.

The first situation arises when pulse width modulator 122 provides a signal for FET shunts 110 to be switched on. This situation is typically also present in a conventional power-rectification circuit. The second situation is proper to the application and ensures that the FET shunt is "on" when a connection is required between FET source 114 connected to the neutral line and the power source, i.e. permanent magnet alternator 100. This is supposed to avoid that the FET shunt is switched off when the current needs a return path to permanent magnet alternator 100, thereby preventing the forced "body-drain" connection of conventional systems.

3. *Admittance of the late-filed claim requests*

The main and first auxiliary request, each comprising a new set of claims and amended pages of the description, were filed in response to objections raised by the board in the communication pursuant to Rule 100(2) EPC (cf. point IV above). In this communication, the board had invited the appellant to address and overcome the deficiencies under Articles 84 and 123(2) EPC, either by amendment of by submitting persuasive arguments.

3.1 As regards claim 1 of the **main request**, one of those objections concerned the following expression A (board's labelling):

A: "[a]n electrical system [including a field effect transistor ... shunt regulator]",

for which the board had considered that the term "electrical system" was an unallowable intermediate generalisation of the "electrical power generating system" of original claim 9 (underlining added by the

board). The board had emphasised that, within the context of the electrical *power generating* system, the term "electrical phases" has a precise meaning for a skilled reader, unlike for a *general* "electrical system". By merely stating that the electrical system comprises a number of electrical phases as in claim 1 of the present main request, this issue is evidently not entirely resolved.

3.1.1 While, as brought forward by the appellant, original claim 1 *does* indicate that the plurality of FET shunts should "equal the number of electrical phases of an electrical system" and thereby *indeed* refers to "an electrical system", this does not mean that original claim 1 by *itself* already suffices as a basis for expression A without having to resort to original claim 9: the "electrical system" referred to in original claim 1 is plainly **not** part of original claim 1. In particular, the "electrical system" does not necessarily comprise the current controlled shunt regulator of original claim 1: it can refer to any electrical system with a plurality of electrical phases.

3.1.2 Contrary to what was implied by the appellant, the Guidelines for Examination, F-IV, 4.14 do not state that a claim directed towards a first entity and referring to a second entity that is not part of a claimed first entity can be (re-)directed towards a combination of those two entities. Rather, it must be verified, for each case individually, whether such a combination falls within the boundaries set by Article 123(2) EPC.

In the present case, the "electrical system" of claim 1 of the main request **mandatorily** includes the "field

effect transistor FET shunt regulator", which cannot be directly and unambiguously derived from original claim 1. In fact, the application as filed only provides a direct and unambiguous basis for a combination of an electrical system with a shunt regulator in the context of an electrical power generating system comprising a multiphase permanent magnet alternator, namely in original claim 9.

3.1.3 Consequently, not all of the issues raised by the board are resolved by claim 1 of the main request.

3.2 As to claim 1 of the **first auxiliary request**, it was, by contrast, readily apparent that the objections raised by the board had been overcome appropriately. The board was also able to establish with minimal effort that the amendments to claim 1 did not introduce any new issues of compliance with respect to Articles 84 and 123(2) EPC. In addition, *prima facie*, the subject-matter of claim 1 appeared to be inventive having regard to the documents cited by the examining division against claim 1 of the refused claim request and did not give rise to new objections (cf. Article 13(1) RPBA 2020).

The high likelihood that the appeal would be allowable if the first auxiliary request - which had been filed upon the board's invitation - was admitted also contributed to procedural economy by avoiding the need for oral proceedings.

3.3 In view of the above, the board used its discretionary power under Article 13(1) RPBA 2020

- not to admit the **main request** into the proceedings;

- to admit the **first auxiliary request** into the proceedings.

4. *First auxiliary request: claim 1 - features*

Claim 1 of the **first auxiliary request** includes the following limiting features (as labelled by the board):

(a) An electrical power generating system comprising a multiphase permanent magnet alternator and a current controlled shunt regulator,
the current controlled shunt regulator comprising:
(b) a rectifier;
(c) a controller;
(d) a plurality of field effect transistor FET shunts equal to the number of electrical phases of the permanent magnet alternator;
(e) wherein each of said FET shunts corresponds to a phase of the permanent magnet alternator and is connected in such a way as to allow power to travel unimpeded between said corresponding phase of said permanent magnet alternator and said rectifier when said FET shunt is off and redirect current from said corresponding phase of said permanent magnet alternator to neutral when said FET shunt is on;
(f) wherein the current controlled shunt regulator further comprises a plurality of comparators, each of which has a comparator input connected to a corresponding phase of said permanent magnet alternator;
(g) wherein each of said comparators is arranged to determine if a phase voltage of the corresponding phase is positive or negative, and is arranged to output a corresponding comparator control signal indicating that a corresponding FET shunt of the plurality of FET shunts should be turned on when

the phase voltage is negative, and to not output the corresponding comparator control signal when the phase voltage of the corresponding phase is positive;

(h) wherein said controller is arranged to output a pulse width modulated controller control signal indicating whether the FET shunts should be turned on;

(i) wherein the current controlled shunt regulator further comprises a plurality of logical OR gates each corresponding to a FET shunt of the plurality of FET shunts;

(j) wherein each OR gate comprises a first input and a second input and is arranged to receive and combine the corresponding comparator control signal as the first input and the pulse width modulated controller control signal as the second input, and to output a FET shunt control signal to a gate of the corresponding FET shunt;

(k) wherein each of said FET shunts is arranged to receive the FET shunt control signal from a corresponding logical OR gate of the plurality of logical OR gates;

(l) wherein said controller is arranged to output the pulse width modulated controller control signal identically to each FET shunt so that all FET shunts are activated simultaneously whenever the controller indicates that the FET shunts should be turned on;

(m) wherein each of said logical OR gates is arranged to output the FET shunt control signal to turn said corresponding FET shunt on whenever either the corresponding comparator control signal as the first input or the pulse width modulated controller control signal as the second input indicate that

the corresponding FET shunt should be turned on.

5. *First auxiliary request: claim 1 - Article 123(2) EPC*

5.1 The following direct and unambiguous basis in the application as filed can be identified for claim 1 of the **first auxiliary request**:

- **feature (a)**: original claims 1 and 9;
- **features (b) to (e)**: original claim 1;
- **feature (f)**: page 3, lines 14 to 17 of the description as filed;
- **feature (g)**: page 3, lines 15 to 17 and 23 to 28 as well as page 5, lines 6 to 12 of the description as filed, together with Figure 1 as filed;
- **feature (h)**: page 3, lines 8 to 13 and lines 26 to 28 as well as page 5, lines 4 to 9 of the description as filed;
- **feature (i)**: original claim 1 and Figure 1 as filed;
- **features (j), (k) and (m)**: page 3, lines 22 to 28, page 4, lines 1 to 7 and page 5, lines 3 to 18 of the description as filed, together with Figures 1 and 2 as filed;
- **feature (l)**: page 3, lines 8 to 13 of the description as filed.

5.10 Claim 1 of the first auxiliary request therefore complies with Article 123(2) EPC.

6. *First auxiliary request: claim 1 - novelty and inventive step*

6.1 Document **D1** is considered to be the most suitable starting point for the assessment of inventive step in the present case. It discloses, in Figures 1 and 10, a

rectifier bridge circuit with diode pairs 21 and 22 as well as 23 and 24 (and, for Figure 10: diode pair 25 and 26) [**feature (b)**] together with switches 32 and 34 (and, for Figure 10: switch 36), which, according to the first sentence of the paragraph bridging pages 2 and 3 can be implemented as MOSFETs - i.e. a special kind of FET - and are, as apparent from the first full paragraph of page 4, connected in shunt across diodes 22 and 24 (and, for Figure 10: across diode 26). The system of Figures 1 and 10 uses a permanent magnet alternator (see page 3, last two full paragraphs) as is the case in the present application [**feature (a)**], where for Figure 10 the number of FET shunts equals the number of phases of the permanent magnet alternator, namely three (see page 6, line 2) [**feature (d)**].

Moreover, there is a control unit (having reference number "3" in the paragraph bridging pages 4 to 5) that opens or closes the switches, i.e. turns them "on" or "off" [**feature (c)** and **feature (h)**, except for "pulse width modulated"]. As apparent from the second half of page 4 and from the circuits in Figures 1 and 10 themselves, power can travel unimpededly from permanent magnet alternator 1 to diodes 21 to 26 when switches 32 to 36 are open, whereas, when the switches are closed, phases 11 to 13 of alternator 1 are connected directly to neutral ("0V") line 5 [**feature (e)**]. The opening and closing of switches 32 to 36 by control unit 3 enables the system to operate in different modes according to the output voltage that is required (see the last full paragraph of page 4 and the paragraph bridging pages 4 and 5).

6.2 Hence, D1 does not disclose

- **features (f) to (g);**

- the part of **feature (h)** that the controller control signal is in pulse width modulated form;
- and **features (i) to (m)**.

6.3 The technical effect attributable to distinguishing features (f), (g), (i) to (k), and (m) is that the forced "body-drain" connection as referred to in point 1 above is avoided. In particular, as per feature (m), the claimed FET shunts are switched on whenever either the corresponding comparator control signal or the pulse width modulated controller control signal indicates that the FET shunt should be turned on. The former control signal input indicates, as apparent from feature (g), that the FET shunt is to be turned on when its corresponding phase voltage is negative, thereby setting the FET shunt in a *conducting* state when current is required to flow from the neutral line back to the phase, as set out in lines 10 to 16 of page 5 of the application as filed.

6.4 In point 2.2 of the decision under appeal, the disclosure of D1 was combined with the teaching of **D2** to arrive at a configuration which would allegedly fall under the scope of the claim. However, D2 does not concern any of the distinguishing features acknowledged above in point 6.2. In particular, the board agrees with the appellant that D2 neither concerns the "comparators" of features (f) and (g) nor the "logical OR gates" of features (i) to (k) and (m). The decision under appeal does not address *why* the skilled person would have implemented comparators and logical OR gates in the configuration of D1.

In this respect, it is emphasised that D2 discloses in points 2.2.1 to 2.2.3 of page 1194 three different methods of MOSFET control, none of which uses logical

OR gates. Of course, comparators and logical OR gates are, *per se,* known to the skilled person based on their common general knowledge and could be present in, for instance, the "commercial circuits" referred to in the last paragraph of point 2.3 of the decision under appeal. However, there would be no reason for the skilled person, other than based on an *ex-post facto* analysis, to adopt the configuration *specifically* defined by features (f), (g), (i) to (k), and (m) in the system resulting from a combination of D1 with D2.

Claim 1 of the first auxiliary request involves therefore an inventive step at least in view of its features (f), (g), (i) to (k), and (m).

6.5 Consequently, claim 1 of the first auxiliary request fulfils the requirements of Articles 54 and 56 EPC.

7. *First auxiliary request: claim 1 - clarity*

Claim 1 now expresses in sufficiently clear language the essential features of the invention and therefore complies with Article 84 EPC.

8. In conclusion, given that the objections which led to the refusal of the present application are overcome, a patent can be granted on the basis of the claims (and of the amended description pages 1, 2 and 2a) of the present first auxiliary request.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following application documents:

   - **Claims 1 to 4** as filed as "first auxiliary request" with the submission dated 10 December 2020;
   - **Description, pages 1, 2 and 2a** as filed as "first auxiliary request" with the submission dated 10 December 2020;
   - **Description, pages 3 to 5** as originally filed;
   - **Drawings, sheet 1/1** as originally filed.

The Registrar: The Chair:

B. Brückner K. Bengi-Akyürek

Decision electronically authenticated