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Datasheet for the decision of 7 July 2021

Case Number: T 1349/17 - 3.5.07

Application Number: 13004992.7

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Language of the proceedings: EN

Title of invention:
NAND flash memory device and method for setting access thereto

Applicant:
Micron Technology, Inc.

Headword:
NAND flash memory/MICRON TECHNOLOGY

Relevant legal provisions:
EPC Art. 76(1), 84, 111(1), 123(2)
RPBA 2020 Art. 11, 12(2), 13(2)

Keyword:

Claims - clarity - main request and first to fourth auxiliary requests (no)
Amendments - added subject-matter - first, fourth, sixth and ninth auxiliary requests (yes)
Amendment after summons - exceptional circumstances - new fifth auxiliary request (no) - exceptional circumstances - new seventh and new eighth auxiliary requests (yes)
Remittal - special reasons for remittal

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Case Number: T 1349/17 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 7 July 2021

Appellant: (Applicant)	Micron Technology, Inc. 800 South Federal Way Boise, ID 83707-0006 (US)
Representative:	Gill Jennings & Every LLP The Broadgate Tower 20 Primrose Street London EC2A 2ES (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 10 January 2017 refusing European patent application No. 13004992.7 pursuant to Article 97(2) EPC**

Composition of the Board:

Chair	J. Geschwind
Members:	P. San-Bento Furtado
	C. Barel-Faucheux

Summary of Facts and Submissions

I. The appeal lies from the decision of the examining division to refuse European patent application No. 13004992.7, filed as a divisional of European patent application No. 08839630.4, for added subject-matter in claim 1 of each of a main request and first and second auxiliary requests. In *obiter dicta* the examining division expressed its opinion that claim 1 of each of the requests lacked inventive step.

II. The following documents were cited in the decision under appeal:

D1: US 2006/0268642 Al, published on 30 November 2006;

D2: Intel: "Intel® 64 and IA-32 Architectures Software Developer's Manual - Volume 3A: System Programming Guide, Part 1", Chapters 8 and 24, May 2007;

D3: US 6 446 177 Bl, published on 3 September 2002.

III. With the statement of grounds of appeal, the appellant filed amended claims of a main request and four auxiliary requests and requested that the decision be set aside and that a patent be granted on the basis of the main request or one of the first to fourth auxiliary requests.

IV. The appellant was invited to oral proceedings. In a subsequent communication sent in advance of the oral proceedings, the board introduced the following document cited in the proceedings of the parent application:

D4: EP 1 764 803 A1, published on 21 March 2007.

The board expressed its preliminary opinion that claim 1 of the main request satisfied the requirements of Articles 76(1) and 123(2) EPC, but not those of Articles 56 and 84 EPC. The subject-matter of claim 1 of the main request did not seem to be inventive when starting from the disclosure of either document D1 or D4. The distinguishing features were known from document D4 and/or common general knowledge illustrated in part by document D2. Claim 1 of the first to fourth auxiliary requests did not fulfil the requirements of Articles 56 and 84 EPC. Claim 1 of the first and fourth auxiliary requests added subject-matter beyond the content of the parent application and the application as filed (Articles 76(1) and 123(2) EPC). Corresponding objections applied to other claims of each of the requests which recited the same or similar subject-matter.

V. With a letter of reply dated 7 June 2021 the appellant filed new sets of claims of fifth to ninth auxiliary requests.

VI. Oral proceedings were held as scheduled by video conference. During the oral proceedings the appellant submitted new fifth, new seventh and new eighth auxiliary requests to replace the fifth, seventh and eighth auxiliary requests. At the end of the oral proceedings, the Chair announced the board's decision.

VII. The appellant's final requests were that the decision under appeal be set aside and that a patent be granted on the basis of the main request, or one of the first to fourth auxiliary requests, all five requests filed with the statement of grounds of appeal, the new fifth auxiliary request filed during the oral proceedings before the board, the sixth or ninth auxiliary requests filed with the letter of 7 June 2021 or the new seventh

or new eighth auxiliary requests filed during the oral proceedings before the board.

VIII. Claim 1 of the main request reads as follows:

"A NAND flash memory device (10) comprising:
a NAND flash memory array (40);.
a special mode enable register (24) comprising a special mode enable bit, wherein the special mode enable register (24) has a specific register address; and
a controller (14) configured to set the special mode enable bit by writing data into the special mode enable register upon receipt of a register write command that includes the specific register address of the special mode enable register (24), and wherein the controller (14) is configured to operate in a special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command comprising a SPI NAND command."

Claim 5 of the main request reads as follows:
"The NAND memory device (10) of claim 1, wherein the special operational mode comprises a one time programmable 'OTP' access mode, a parameter page access mode, or a block lock access mode, or any combination thereof."

IX. Claim 1 of each of the first, second, third and fourth auxiliary requests differs from claim 1 of the main request, respectively, in that the following text has been added at the end:
(ar1) ", and the special operational mode comprises a one time programmable 'OTP' access mode, a parameter page access mode, or a block lock access mode, or any combination thereof";

(ar2) ", and the special operational mode comprises a parameter page access mode";

(ar3) ", and the special operational mode comprises a one time programmable 'OTP' access mode";

(ar4) ", and the special operational mode comprises a block lock access mode".

X. Claim 1 of the new fifth auxiliary request differs from claim 1 of the main request in that the text at the end of the claim starting with "a controller (14) configured to set the special mode enable bit [...]" has been replaced with the following text:

"a controller (14) configured to operate differently despite receiving the same shared ordinary commands depending on whether the special mode enable bit of the special mode enable register (24) has been set, and wherein the controller (14) is configured to set the special mode enable bit upon receipt of a register write command that includes the specific register address of the special mode enable register (24) to enter a special operational mode of the controller (14), and wherein the controller (14) is configured to operate in the special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command."

Claim 5 of the new fifth auxiliary request reads as follows:

"The NAND memory device (10) of claim 1, wherein the special operational mode comprises a one time programmable 'OTP' access mode, or a parameter page access mode."

XI. Claim 1 of the sixth auxiliary request differs from claim 1 of the first auxiliary request in that the text "a controller (14) configured to set the special mode

enable bit [...] comprising a SPI NAND command" has been replaced with the following text:

"a controller (14) configured to set the special mode enable bit upon receipt of a register write command that includes the specific register address of the special mode enable register (24) to enter a special operational mode of the controller (14), and wherein the controller (14) is configured to operate in the special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command".

XII. Claim 1 of the ninth auxiliary request differs from claim 1 of the sixth auxiliary request in that the text (ar1) (see section IX. above) has been replaced with a text corresponding to the text of (ar4) where the indefinite article "a" has been deleted.

XIII. Claim 1 of the new seventh auxiliary request reads as follows:

"A NAND flash memory device (10) comprising:

a NAND flash memory array (40);

a special mode enable register (24) comprising a special mode enable bit, wherein the special mode enable register (24) has a specific register address; and

a controller (14) configured to operate differently despite receiving the same shared ordinary commands depending on whether the special mode enable bit of the special mode enable register (24) has been set, and wherein the controller (14) is configured to set the special mode enable bit upon receipt of a register write command that includes the specific register address of the special mode enable register (24) to enter a special operational mode of the

controller (14), and wherein the controller (14) is configured to operate in the special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command, and the special operational mode comprises parameter page access mode."

Claim 2 of the new seventh auxiliary request reads as follows:
"The NAND memory device of claim 1, wherein the controller (14) is configured to communicate with a master over a serial peripheral interface protocol."

Claim 3 of the new seventh auxiliary request reads as follows:
"A method of operating a NAND flash memory device (10) comprising a special mode enable register (24) that has a specific address and a controller (14), wherein the controller (14) is configured to operate differently despite receiving the same commands depending on whether a special mode enable bit of the special mode enable register (24) has been set, the method comprising:

setting the special mode enable bit in the special mode enable register of the flash memory device (10) to cause the flash memory device (10) to exit an ordinary operational mode and to enter a special operational mode, whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command, wherein setting the special mode enable bit comprises sending a register write command signal (82) to a data input pin of the flash memory device (10), sending a register address signal (84) to the data input pin of the flash memory device (10), and sending a data signal (86) to

the data input pin of the flash memory device (10), wherein the register address signal includes the specific register address of the special mode enable register;

performing one of the respective special operations in the special operational mode by issuing the shared ordinary commands; and

resetting the special mode enable bit in the special mode enable register (24) of the flash memory device (10) to cause the flash memory device 10)[sic] to exit the special operational mode and to re-enter the ordinary operational mode;

wherein setting the special mode enable bit in the special mode enable register (24) of the flash memory device to cause the flash memory device (10) to exit the ordinary operational mode and to enter the special operational mode comprises setting a parameter page access mode enable bit in a parameter page access mode enable register (24) of the flash memory device (10) to cause the flash memory device (10) to exit the ordinary operational mode and to enter a parameter page access mode."

Claim 4 of the new seventh auxiliary request reads as follows:

"The method of claim 3, wherein performing the respective one of the special operations in the special operational mode by issuing the shared ordinary commands comprises performing a parameter page access operation in the parameter page access mode by issuing a page read command, a read status command, and/or a random data read command."

XIV. Claim 1 of the new eighth auxiliary request differs from claim 1 of the new seventh auxiliary request in that the text "comprises parameter page access mode" at

the end of the claim has been replaced with "comprises a one time programmable 'OTP' access mode".

XV. The appellant's arguments, where relevant to this decision, are addressed in detail below.

Reasons for the Decision

Application

1. The application concerns a NAND flash memory device configured for interconnection via a serial peripheral interface (SPI)(see paragraph [0001] of the description as originally filed), which supports additional "special operations" by using "shared ordinary commands" in a special operational mode rather than introducing additional commands exclusively for performing those special operations (paragraph [0041], page 17, lines 3 and 4).

1.1 When the memory controller enters the special operational mode, shared ordinary commands, such as page read, read status, or random data read, are used to perform a new operation to achieve a result not possible in an "ordinary operational mode" (paragraph [0041]).

1.2 Special operations may be, for example, parameter page operations (paragraphs [0041] and [0043], Figure 7) or one time programmable (OTP) memory operations (paragraph [0049]). Each page of an OTP block may be written on a fixed number of times, typically one to four times, before a page lock bit is set, permanently locking the page from modification (paragraphs [0036], [0047] to [0051], Figures 8 and 9).

Main request

2. Claim 1 recites a NAND flash memory device comprising:

(a) a NAND flash memory array;.

(b) a special mode enable register comprising a special mode enable bit, wherein the special mode enable register has a specific register address; and

(c) a controller configured to set the special mode enable bit by writing data into the special mode enable register upon receipt of a register write command that includes the specific register address of the special mode enable register, and wherein the controller is configured to

(c1) operate in a special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in response to a received shared ordinary command comprising a SPI NAND command.

3. *Clarity and claim interpretation - claim 1*

3.1 From features (b) and (c) of claim 1 it is not clear what the purpose of the "special mode enable bit" is nor when the controller enters the special operational mode.

3.2 The expressions "special mode enable register" and "special mode enable bit" of claim 1 are not mentioned in the first part of the description and are used for the first time in the following passage of clause 10 on pages 16 and 17 (where clause 10 corresponds to original claim 10 of the parent application):

> "setting a special mode enable bit in a special mode enable register of a flash memory device to cause the flash memory device to exit an ordinary operational mode and to enter a special operational

mode, the ordinary operational mode and the special operational mode having a plurality of shared commands associated therewith, wherein each of the plurality of shared commands is associated with performing an ordinary operation for the ordinary operational mode and a special operation for the special operational mode".

From this passage, read in the context of the whole description, the board concludes that the "special mode enable register" is a generalisation of the "parameter page access register" and "OTP enable register" described for instance in paragraphs [0042] and [0046].

Similarly, the "special mode enable bit" is a generalisation of the enable bit of those two registers, which are also referred to in the description as "parameter page (access) enable bit" (see paragraphs [0042], [0044]), and "OTP enable bit" (see paragraphs [0048] and [0052]).

3.3 At the oral proceedings, the appellant agreed with the board's interpretation of claim 1.

In its reply to the board's clarity objection, the appellant submitted that claim 1 specified that the special mode enable bit was set by writing data into the special mode enable register as explained in feature (c). Therefore, the claim clearly set out what the purpose was and how the controller was configured to set the special mode enable bit. At the oral proceedings, the appellant also submitted that it was clear that the special mode enable bit was used to change mode.

The board does not find the appellant's arguments convincing. Even though the skilled person could be expected to assume that the "special mode enable bit" is somehow related with the "special operational mode", they would still not be able to confirm unambiguously from the text of claim 1 that that is the case, nor to obtain from the claim exact information about what happens when the special mode enable bit is set by the controller, for which purpose it is set, or how the special mode enable bit and the special operational mode are related. In particular, the claim does not specify that the special mode enable bit is set to cause the flash memory device to enter the special operational mode described in feature (c1).

3.4 Therefore, claim 1 of the main request is unclear and does not satisfy the requirements of Article 84 EPC.

First to fourth auxiliary requests

4. Compared to claim 1 of the main request, claim 1 of the first to fourth auxiliary requests further specify features (ar1) to (ar4) listed in section IX. above.

5. *Clarity - claim 1 of first to fourth auxiliary requests*

5.1 Features (ar1) to (ar4) merely add that the special operational mode comprises one or more of the following modes: "one time programmable 'OTP' access mode", "parameter page access mode", or "block lock access mode". These features do not contribute to clarify the purpose of the "special mode enable bit" and how it relates to the "special operational mode".

5.2 In view of that, the objection raised above with regard to claim 1 of the main request applies equally to claim 1 of each of the first to fourth auxiliary

requests, which hence do not fulfil the requirements of Article 84 EPC.

6. *Clarity, support and added subject-matter - claim 1 of first and fourth auxiliary requests*

6.1 The description of the present application discloses a "parameter page access mode" in paragraphs [00040] to [00044] with reference to Figure 7, and an "OTP block access mode" in paragraphs [00045] to [00053] with reference to Figure 9. In the context of the method of Figure 10, two modes are mentioned: the "OTP block access mode", as described in paragraphs [00054] to [00057], and the "OTP write protect mode" mentioned in paragraph [00056]. Original claims 17 and 18 of the parent application, which correspond to clauses 17 and 18 of page 18 of the present application, specify a "one time programmable (OTP) block page lock mode".

However, there is no disclosure of a "block lock access mode" (see features (ar1) and (ar4) above) in the application and in the parent application as originally filed and it is not clear whether that mode is intended to correspond to the "OTP write protect mode" or one of the other modes mentioned in the application.

6.2 The appellant argued that paragraphs [0023] and [0024] of the application as originally filed provided a basis for the "block lock access mode" in that it described registers used in conjunction with device operation, particularly a block writing lock register to prevent certain portions of memory from being written to, in addition to an OTP enable register to enable reading from or writing to an OTP portion of memory, and/or a parameter page enable register to enable reading from or writing to a parameter page of memory. The appellant submitted that the "block writing lock register" of

paragraph [0023] corresponded to the "block lock access mode" of (ar1) and (ar4).

The appellant's arguments are not convincing. Paragraph [0023] describes the "block writing lock register" as being used to "prevent certain portions of memory from being written to" and as an access register 24. Paragraphs [0023] to [0025] explain that an enable bit might be set for a given register to change the controller to an "alternative operational mode" and that a user can use the access registers to control many functional aspects of the memory device. Examples are given of such functional aspects in paragraph [0025], but they are not related to the function of the "block writing lock register". Paragraphs [0023] to [0025] do not disclose that setting of a bit of the "block writing lock register" causes the controller to change to another operational mode, or that preventing memory portions from being written to is implemented by a change to another operational mode, and there is no other description of the "block writing lock register" in the application.

There is hence no reason for the skilled person to assume, based on the text of the claim and of paragraph [0023], that the "block lock access mode" of claim 1 of the first and fourth auxiliary requests is related to the "block writing lock register" of paragraph [0023]. In addition, even if the two features were recognised as being related, there would be no basis for combining either feature with the other features of claim 1 of the first and fourth auxiliary requests.

6.3 At the oral proceedings the appellant further cited Figure 10 as a basis for the combinations of features

including the "block lock access mode" of claim 1 of the first and fourth auxiliary requests.

Figure 10 illustrates a "technique for preventing writing to (i.e., locking) a page of one time programmable (OTP) memory". It is described in paragraphs [0054] to [0057], in which an "OTP block access mode" and an "OTP write protect mode" are disclosed.

In the board's view, it is not clear that the "block lock access mode" of (ar1) and (ar4) corresponds to one of the two OTP modes described in Figure 10. Furthermore, if the board accepted that argument, then it would not be clear to which OTP modes of the description the "OTP access mode" of (ar1) corresponded, and there would be no basis for combining the "OTP access mode" with the "block lock access mode" in (ar1) and no basis for omitting the OTP character of the access mode in feature (ar4).

6.4 For those reasons, the feature "block lock access mode" of claim 1 of the first and fourth auxiliary requests is unclear and not disclosed in the application, nor the parent application, as originally filed, let alone in combination with features (c) and (c1), or in combination with the other two modes of feature (ar1).

Claim 1 of the first and fourth auxiliary requests are thus unclear, lack support by the description, and go beyond the content of the application and parent application as filed (Articles 84, 76(1) and 123(2) EPC).

New fifth auxiliary request

7. The new fifth auxiliary request was submitted during the oral proceedings to replace the then fifth auxiliary request.

8. *Admissibility of the request*

8.1 The new fifth auxiliary request was submitted at the oral proceedings and therefore after the period mentioned in Article 13(2) RPBA 2020. It thus classifies as an amendment to a party's appeal case which shall, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned.

8.2 At the oral proceedings, the appellant argued that the new fifth auxiliary request should be admitted because it had been filed to overcome an objection raised for the first time during the oral proceedings against claim 5 of the fifth auxiliary request then on file, where claim 5 was identical to claim 5 of the main request (the text of claim 5 of the main request and new fifth auxiliary request is reproduced in sections VIII. and X. above).

8.3 However, the objection that the board raised at the oral proceedings against claim 5 of the fifth auxiliary request then on file was based on a feature corresponding to feature (ar1) of the first auxiliary request (see section IX. above). The same objection had already been raised in the board's communication against the almost identical feature (ar1) of claim 1 of the first auxiliary request. Even though in its communication the board had not raised that objection against claim 5 of the main request, the appellant

should have expected the same objection to be raised against claims covering identical or similar subject-matter (which did not have to be, but was, mentioned in the board's communication, see point 18 of that communication).

8.4 In view of this, the board does not recognise any exceptional circumstances justifying admittance of the request in such a late stage and does not admit the new fifth auxiliary request into the proceedings (Article 13(2) RPBA 2020).

Sixth and ninth auxiliary requests

9. *Admissibility of the requests*

9.1 The sixth and ninth auxiliary requests were based on the first and fourth auxiliary requests, respectively, and were filed in reply to the board's communication.

Since the two requests were filed before the expiry of the period specified in the board's communication in an attempt to address the objections raised by the board for the first time in that communication, the board accepts that special circumstances under Article 13(2) RPBA 2020 present themselves to admit the two requests. Therefore, the sixth and ninth auxiliary requests are admitted into the proceedings.

10. *Clarity and added subject-matter - claim 1 of sixth and ninth auxiliary requests*

10.1 Claim 1 of the sixth auxiliary request recites feature (ar1) of the first auxiliary request and claim 1 of the ninth auxiliary request specifies that "the special operational mode comprises block lock

access mode" which essentially corresponds to feature (ar4) of the fourth auxiliary request.

10.2 As explained under point 6. above, features (ar1) and (ar4) are unclear, not supported by the description and add subject-matter beyond the disclosure of the application as filed. The same reasoning applies to the corresponding features of claim 1 of the sixth and ninth auxiliary requests.

10.3 Therefore, claim 1 of the sixth and ninth auxiliary requests do not satisfy the requirements of Articles 84, 76(1) and 123(2) EPC.

New seventh and new eighth auxiliary requests

11. Claim 1 of the new seventh auxiliary request differs from claim 1 of the main request in that features (c) and (c1) have been replaced with the following features (itemisation added by the board):

(d) "a controller (14) configured to operate differently despite receiving the same shared ordinary commands depending on whether the special mode enable bit of the special mode enable register (24) has been set, and wherein

(d1) the controller (14) is configured to set the special mode enable bit upon receipt of a register write command that includes the specific register address of the special mode enable register (24) to

(d2) enter a special operational mode of the controller (14), and wherein the controller (14) is configured to

(d3) operate in the special operational mode whereby a new operation is performed to achieve a result not possible in an ordinary operational mode in

response to a received shared ordinary command, and

(d4) the special operational mode comprises parameter page access mode."

Feature (d1) is an amended version of feature (c), feature (d3) corresponds to feature (c1) amended to delete the reference to a SPI NAND command. Feature (d4) corresponds essentially to feature (ar2).

12. Claim 1 of the new eighth auxiliary request differs from claim 1 of the new seventh auxiliary request in that "comprises parameter page access mode" in (d4) has been replaced with "comprises a one time programmable 'OTP' access mode" (which corresponds to feature (ar3)).

13. *Admissibility of the requests*

13.1 The new seventh and new eighth auxiliary requests were filed at the oral proceedings before the board to replace the seventh and eighth auxiliary requests then on file. The two new requests were filed after the board informed the appellant that the claims of the then seventh and eighth auxiliary requests overcame the objections raised in the board's communication with regard to Articles 84, 76(1) and 123(2) EPC, but that some minor corrections were required which had not been mentioned before.

The seventh and eighth auxiliary requests were based on the second and third auxiliary requests and had been filed before the expiry of the period specified in the board's communication in order to address the objections raised for the first time in that

communication. The seventh and eighth auxiliary requests were therefore admissible.

13.2 In view of the above, and especially since the new seventh and new eighth auxiliary requests were filed to overcome objections raised for the first time during the oral proceedings against admissible requests, special circumstances under Article 13(2) RPBA 2020 present themselves for admitting the two new requests. Therefore, the new seventh and new eighth auxiliary requests are admitted into the proceedings.

14. *Clarity and support - new seventh auxiliary request*

14.1 Claim 1 overcomes the lack of clarity objections raised against the main request (see point 3.3 above) and other requests. In particular, the claim now explains in unambiguous terms in features (d1) and (d2) that the controller enters a special operational mode when the special mode enable bit is set, and in features (d) and (d3) that the controller operates differently for the same shared ordinary commands depending on the special mode enable bit being set. It is therefore clear that the purpose of the special mode enable bit is to determine in which of the two different modes the controller operates, and that the controller changes mode when the special mode enable bit is set.

14.2 The same applies to independent claim 3, which specifies a method of operating a NAND flash memory device in similar terms to that of claim 1.

14.3 The board is therefore satisfied that the new seventh auxiliary request meets the requirements of Article 84 EPC.

15. *Added subject-matter - new seventh auxiliary request*

15.1 In the decision under appeal, refusal was based on the ground that there was no basis in the application as filed for the feature "accessing a second portion of the flash memory array (40) separate from the first portion of the flash memory (40)". Such an objection no longer applies because the feature is not recited in the claims.

15.2 Claim 1 describes a NAND flash memory device (10) comprising a NAND flash memory array (40), a register (24) and a controller (14) (features (a) to (d)). These features are based on paragraphs [00020], [00021] and [00023], and Figure 1, of the application as filed.

The other features of claim 1 are disclosed in paragraphs [00040] to [00044] with reference to Figure 7, which describe the "parameter page access mode". In particular, paragraph [00041] discloses the operation of the controller in the "special operational mode" as specified in features (d) and (d3), and paragraph [0042] describes setting the "page enable bit" to cause the controller to enter the "parameter page access mode" by issuing a register write command as described in features (d), (d1), (d2) and (d4).

The term "special mode enable register" was not used in the application as filed, but it is clear for the skilled person that it corresponds to one of the registers mentioned in paragraph [00023] and to the "parameter page access register" disclosed in paragraph [00042] with regard to the embodiment of Figure 7. Similarly, the "special mode enable bit" corresponds to the "enable bit" mentioned in several passages, including paragraph [00042], and to the

"parameter page enable bit" of the embodiment of Figure 7.

15.3 Independent method claim 3 recites a method of operating a NAND flash memory device in terms similar to those of claim 1 and further adds the features specifying that "setting the special mode enable bit comprises sending a register write command signal (82) to a data input pin of the flash memory device (10), sending a register address signal (84) to the data input pin of the flash memory device (10), and sending a data signal (86) to the data input pin of the flash memory device (10), wherein the register address signal includes the specific register address of the special mode enable register". These features are disclosed in paragraphs [0030] to [0034] and Figures 3 and 4 of the application as originally filed.

15.4 The features of claim 2 are described for instance in paragraphs [00020] and [00041] and the subject-matter of claim 4 finds a clear basis in paragraph [00041].

15.5 Therefore, the board is satisfied that the new seventh auxiliary request meets the requirements of Article 123(2) EPC.

15.6 Since the content of this and the parent applications as originally filed is the same, the new seventh auxiliary request also meets the requirements of Article 76(1) EPC.

Concluding remarks and remittal

16. In the decision under appeal the application was refused for added subject-matter. That ground for refusal cannot be upheld for the new seventh auxiliary

request, which satisfies the requirements of Articles 76(1), 84 and 123(2) EPC.

17. The examining division gave its opinion on inventive step in an *obiter dictum* but did not decide on the question. The board has introduced a new prior-art document into the proceedings and the claims have been amended in the appeal proceedings. Under these circumstances, assessment of the new claims with regard to inventive step should more appropriately be done by the examining division as the primary object of the appeal proceedings is to review the decision under appeal in a judicial manner (Article 12(2) RPBA 2020). These are special reasons for remitting the case for further prosecution (Article 11 RPBA 2020).

In accordance with Article 111(1) EPC, the case is thus to be remitted for further prosecution on the basis of the new seventh and new eighth auxiliary requests, so that inventive step of the claims can be fully assessed by the department of first instance.

18. The board notes that minor obvious corrections to the claims of the new seventh and new eighth auxiliary requests may be necessary. For example, in the new seventh auxiliary request the appellant may want to correct the text "the special operational mode comprises parameter page access mode" to "the special operational mode comprises a parameter page access mode" in claim 1 and insert "(" before "10)" in the text "to cause the flash memory device 10)" of claim 3.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division for further prosecution on the basis of the new seventh and new eighth auxiliary requests.

The Registrar: The Chair:

S. Lichtenvort J. Geschwind

Decision electronically authenticated