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Datasheet for the decision of 14 April 2021

Case Number: T 1381/17 - 3.4.03

Application Number: 07778530.1

Publication Number: 1994553

IPC: H01L21/28

Language of the proceedings: EN

Title of invention:
GATE-COUPLED EPROM CELL FOR PRINTHEAD

Applicant:
Hewlett-Packard Development Company, L.P.

Headword:

Relevant legal provisions:
EPC 1973 Art. 54(1), 56, 84
EPC Art. 123(2)

Keyword:
clarity - (yes)
added subject matter - (no)
novelty - (yes)
inventive step - (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
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Beschwerdekammern

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Case Number: T 1381/17 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 14 April 2021

Appellant: (Applicant)	Hewlett-Packard Development Company, L.P. 10300 Energy Drive Spring TX 77389 (US)
Representative:	Stöckeler, Ferdinand Schoppe, Zimmermann, Stöckeler Zinkler, Schenk & Partner mbB Patentanwälte Radlkoferstrasse 2 81373 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 14 February 2017 refusing European patent application No. 07778530.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Papastefanou
	W. Van der Eijk

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing the European patent application No. 07 778 530.1 (published as WO 2007/120988 A2) on the grounds that the main request before it lacked clarity (Article 84 EPC 1973) and contained subject-matter extending beyond the originally filed application (Article 123(2) EPC). Auxiliary Requests 1 to 3, which were filed two days before the oral proceedings before the examining division, were not admitted into the procedure under Rule 137(3) EPC because the division considered them to be late filed and *prima facie* not allowable.

II. Reference is made to the following document, cited during the first instance examination procedure:

D1: GB 2 320 807 A.

III. The appellant (applicant) requested that the decision under appeal be set aside and that a patent be granted on the basis of the Main Request underlying the decision under appeal. Alternatively, the appellant requested that a patent be granted on the basis of one of the First to Third Auxiliary Requests. The First and Second Auxiliary Requests correspond respectively to Auxiliary Requests 1 and 2 that were not admitted by the examining division and the Third Auxiliary Request was filed with the statement of the grounds of appeal.

IV. Following a communication from the board, the appellant filed amended description pages with a letter dated 17 September 2020. The Main Request is currently composed as follows:

- Description, Pages 1-3, 3a, and 4-25, filed with letter of 17 September 2020;
- Claims 1 to 6, filed with letter of 19 December 2016;
- Drawings, Sheets 1/6 to 6/6 as published.

V. Claim 1 of the Main Request has the following wording:

A printhead control circuit for an inkjet printer, the printhead control circuit comprising an EPROM cell (270), the printhead control circuit having a semiconductor substrate (252), one and only one polysilicon layer (256) disposed above the semiconductor substrate (252), and a conductive layer (260) disposed above the polysilicon layer (256), the EPROM cell (270) comprising:

a control transistor (272), having a floating gate (280) comprising a portion of the polysilicon layer (256);

an EPROM transistor (274), having a floating gate (282) comprising a portion of the polysilicon layer (256); and

an electrical interconnection, comprising a portion of the conductive layer (260) interconnecting the floating gate (280) of the control transistor (272) and the floating gate (282) of the EPROM transistor (274),

wherein the control transistor (272) comprises a source (278) and a drain (276), and the EPROM transistor (274) comprises a drain (284),

wherein the conductive layer (260) is configured to connect the source (278) of the control transistor (272) to the drain (284) of the EPROM transistor (274).

VI. The wording of the claims of the auxiliary requests is not relevant for this decision.

VII. The appellant argued essentially that the interpretation of the claims by the examining division did not correspond to how a skilled person would interpret them and therefore the claims of the Main Request were clear and did not contain added subject-matter.

Reasons for the Decision

1. The appeal is admissible.

2. The claimed invention

The invention relates to an EPROM (Erasable Programmable Read Only Memory) cell for an inkjet printhead.

Ink cartridges for inkjet printers carry their own printhead and memory cell. It is necessary for each ink cartridge to provide the printer controller with information such as the type of ink it contains, use parameters of the printhead, etc. so that the printer controller can integrate the cartridge in the operation of the printer and operate it properly.

Memory cells for printheads are normally read-only memories (ROM), since the printer controller does not need to write any data on them. During manufacture of the ink cartridge, the memory cells are written with the necessary information and this is done with some form of programming of the cell (Programmable ROM - PROM). An early type of such PROM cells used fuses. The fuses were selectively burnt (with high electrical

charge) and the combination of burnt and not burnt fuses provided the necessary information (a burnt fuse corresponded to 0, a not burnt fuse to 1). Disadvantages of such cells included size (the fuses were rather large with respect to the overall dimensions), the risk to damage the rest of the cell when burning a fuse and the fact that it was not possible to correct any error since a burnt fuse could not be recovered.

Erasable PROMs (EPROMs) are read-only memory cells that can be erased and reprogrammed. They use transistors for storing charge on their gates. A high charge corresponds to 1 and a low charge to 0. EPROMs were used in inkjet printheads as a replacement to the PROMs with fuses. There are two main issues with such EPROM cells, the chip of the cell requires more layers than conventional PROM cells and this affects its size and complicates its manufacture, and the charge at the transistors decreases with time, i. e. they lose the information written in them (see page 2, line 4 to page 3, line 20 of the application as published).

The claimed circuit proposes a simplified structure with fewer layers and improved electrical characteristics (i. e. memory life-time). This is achieved by increasing the capacitive coupling between the control node and the floating gate. Capacitive coupling is also increased by connecting the source of the control transistor to the drain of the EPROM transistor through a conductive layer (see page 16, lines 18 to 31). By this connection, a more efficient space layout of the cell can be obtained, simplifying the manufacture of the cell and reducing its size (see page 17, lines 7 to 14).

3. Main Request

3.1 Clarity (Article 84 EPC 1973)

3.1.1 The examining division held that claim 1 of the Main Request lacked clarity.

According to the examining division, the formulation of the feature *"wherein the conductive layer is configured to connect the source of the control transistor to the drain of the EPROM transistor"* (last feature of claim 1), in particular the use of the expression "configured to", left open whether the conductive layer was electrically connecting the source of the control transistor to the drain of the EPROM transistor or whether it was arranged to electrically connect the source of the control transistor to the drain of the EPROM transistor, e. g. by an unspecified switching means. The feature was thus unclear for the skilled person (see point 1 of the grounds of the contested decision)

3.1.2 The board does not agree with the examining division's interpretation of this feature. The term "configured to" is standard terminology in patent applications and is to be understood as "capable of". A device that is configured to do something means that it can do it.

In the board's view, the skilled person reads the claim with a will to understand. The definition of the claim makes it sufficiently clear that the conductive layer connects the source of the control transistor to the drain of the EPROM transistor. The term "configured to" is to be understood as indicating that the conductive layer (260) is fabricated and placed within the claimed printhead control circuit in such a way that it can

connect the source (278) of the control transistor (278) to the drain (284) of the EPROM transition ("74).

There is no hint in the claim of any other (type of) connection between the source of the control transistor and the drain of the EPROM transistor and the skilled person has no reason to contemplate any other way of implementing this connection. Moreover, the board cannot follow the examining division's interpretation that the conductive layer may be configured to provide a connection between the source of the control transistor and the drain of the EPROM transistor via another device, like an unspecified switching means, since no hint in this direction is to be found in the claims or in the application as a whole. In the board's view, if the claim defines that the conductive layer is configured to connect the source of the control transistor to the drain of the EPROM transistor, then it is clear that it is the conductive layer that provides this connection.

3.1.3 In the board's view, therefore, claim 1 of the Main Request is clear (Article 84 EPC 1973).

3.1.4 In addition, with the amendments carried out in the description, the objection for lack of clarity raised by the board in its communication of 13 August 2020 (point 2) has been overcome.

3.2 Added subject matter (Article 123(2) EPC)

3.2.1 According to the examining division, there was no disclosure in the originally filed application of a conductive layer that connected the floating gate of the control transistor to the floating gate of the EPROM transistor and at the same time connecting the

source of the control transistor to the gate of the EPROM transistor. In addition, there was no basis for the combinations of the features of the dependent claims 2 to 6 with the feature of claim 1 according to which the conductive layer was configured to connect the source of the control transistor to the drain of the EPROM transistor (see point 2 of the reasons of the decision under appeal).

3.2.2 The board cannot follow the examining division in this reasoning.

The application describes that the floating gate regions in the polysilicon layer 256 (i. e. the floating gates of the control transistor and the EPROM transistor) *"can be electrically connected by the Metal1 layer 260"*. Moreover, *"[t]he Metal1 layer 260 can be configured to connect the source of the control transistor 272 (Control2, 278) to the drain of the EPROM transistor 274 (Drain 284)."* (see page 16, lines 18 to 27, Figures 7 and 8 of the published application). In the board's view, these passages support the corresponding features of claim 1.

3.2.3 The examining division held that claim 1 defined that the conductive layer was connecting (or was configured to connect) the floating gates of the two transistors to each other and to the source of the control transistor and to the drain of the EPROM transistor, so that all four of these elements would be connected to each other (point 2.4.1 of the grounds of the impugned decision).

The board does not agree with this interpretation. The board agrees with the appellant that a skilled person would know that such a structure (all four elements

connected to each other) would render the claimed control circuit non-functional (page 5, second to fourth paragraphs of the statement of the grounds of the appeal). In the board's view, it is common general knowledge in the art that layers that are grown/placed over a substrate in order to manufacture an electronic circuit are patterned according to the specific circuit design. The skilled person would readily understand that the Metal1 layer 260 in Figure 7 will be patterned so that it can implement a connection between the floating gates of the two transistors and a different, separate connection between the source of the control transistor and the drain of the EPROM transistor. This is also implied in the application, where it is mentioned that the two metal layers (260, 264) provide the conductors for all the necessary circuit connections (lines 14 and 15 on page 15 of the published application).

3.2.4 Furthermore, the board finds that the combinations of the features of claim 1 with the dependent claims are supported by the originally filed application, as well (cited passages below refer to the application as published).
Support for claim 2 can be found in original claim 2, as well as, on page 17, line 12.
Support for claim 3 can be found in original claim 3 and on page 17, lines 15 to 18. Support for claim 4 can be found in original claim 8 and on page 17, lines 27 to 31. Support for claim 5 is to be found in original claim 9, in Figure 10, and on page 20, lines 24 to 29. Support for claim 6 is to be found in original claim 10, as well as Figures 9 and 10, and on page 20, line 30 to page 21, line 30.

3.2.5 The Main Request, hence, fulfills the requirements of Article 123(2) EPC.

3.3 Novelty and Inventive Step (Articles 54(1) and 56 EPC 1973)

3.3.1 In the decision under appeal there is no objection under Articles 54(1) or 56 EPC 1973. The examining division raised such objections in the annex to the summons to oral proceedings (see examining division's letter of 11 May 2016, points 3 and 4).

The board notes that these objections of the examining division related to a different set of claims (filed on 6 February 2015) than the current Main Request. Comparing, however, claim 1 of that set of claims to claim 1 of the Main Request, the board notes that they are very similar. In the board's view, those objections would also apply to the claims of the Main Request and it is appropriate for the board to address them.

It is to be noted, however, that the last feature of claim 1 as filed on 6 February 2015 comprised two alternatives for the connection of the source of the control transistor to the drain of the EPROM transistor, either through a conductive layer or through a resistor. Claim 1 of the Main Request is limited only to the alternative related to the connection through the conductive layer.

3.3.2 The examining division based its objections on document D1. D1, which makes no reference to an inkjet printer or to a printhead for such a printer, describes a flash memory cell, consisting of two transistors T1 and T2 (see Figure 2B). T1 is taken to correspond to the control transistor of claim 1 and T2 to the EPROM

transistor. The floating gates of the two transistors (15A and 15B) are connected via a conductive film 18 (see also page 5, second paragraph). According to D1, the layer 11B is a silicon film, which is locally injected with impurities in order to create channel regions 13A and 13B (see last paragraph on page 4). The examining division held that the region of the silicon film 11B, which is between the source region (12A) of T1 and the drain region (12D) of T2, provided a resistive connection between the two and considered, thus, that this corresponded to the last feature of claim 1.

3.3.3 As explained previously (point 3.3.1 above) according to the last feature of claim 1 of the Main Request, it is the conductive layer that connects the source of the control transistor to the drain of the EPROM transistor. Although there is an embodiment described in the application with a connection using a resistor (see page 17, lines 21 to 26 and Figure 8 of the application as published), the current claim definition is limited to the embodiment whereby the connection is provided by the conductive layer (Metal1, 260).

In the board's view, D1 discloses the alternative related to the connection through a resistor but it is evident that this connection is not the same as a connection through the conductive layer as in claim 1 of the Main Request.

Hence, besides the fact that D1 does not disclose any printhead control circuit for an inject printer, it does not disclose the last feature of claim 1 of the Main Request, either. The subject-matter of claim 1 of the Main Request is, thus, new (Article 54(1) EPC

1973).

3.3.4 This latter distinguishing feature (i. e. the conductive layer is configured to connect the source of the control transistor to the drain of the EPROM transistor) provides for a capacitive coupling of both the source and the drain to the floating gate. This increases the coupling voltage to the floating gate and renders easier the flow of electrons to the floating gate. This improves the electrical characteristics of the circuit, in particular the life-time of the memory cell (see page 16, lines 1 to 31 of the published application).

Starting from D1, the skilled person is thus faced with the problem of how to improve the electrical characteristics of the memory cell.

3.3.5 There is no hint of such an issue in D1. D1 relates to simplifying the manufacturing of the circuit for the memory cell (see for example page 8, first paragraph) and there is no hint for the skilled person to use the conductive film 18 to connect the drain of the source of the control transistor (T1) to the drain of the EEPROM transistor (T2), especially since D1 relates to a memory cell built on an SOI structure. The connection is already established by the portion of the Si layer 11B between 12A and 12D; there would be no reason to use a conductive film to do this.

3.3.6 None of the prior art documents cited in the impugned decision discloses or suggest such a feature, either.

3.3.7 The board notes that the examining division's objection for lack of inventive step against the claims filed on 6 February 2015 related to claim 9, which defined the

use of the memory cell in a printhead control circuit (point 4). In the current Main Request this feature is included in claim 1.

The board agrees with the examining division that the use of the EPROM cell of D1 in a printhead control circuit for an inkjet printer would be an obvious step for the skilled person according to specific needs and circumstances. However, as stated in points 3.3.3 to 3.3.5 above, the board sees at least a further distinguishing feature of the claimed invention over D1, which is not obvious for the skilled person.

3.3.8 The conclusion is that the subject-matter of claim 1 of the Main Request involves an inventive step within the meaning of Article 56 EPC 1973.

4. The board concludes, therefore, that the application according to the Main Request and the invention to which it relates meet the requirements of the EPC and EPC 1973 and a European patent is to be granted according to Article 97(1) EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent in the following version:

   - Description, Pages 1-3, 3a, and 4-25, filed with letter of 17 September 2020;
   - Claims 1 to 6 of the Main Request, filed with letter of 19 December 2016;
   - Drawings, Sheets 1/6 to 6/6 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated