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Datasheet for the decision of 7 September 2021

Case Number: T 1983/17 - 3.4.03

Application Number: 03784733.2

Publication Number: 1523766

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Language of the proceedings: EN

Title of invention:
STRAIN COMPENSATED SEMICONDUCTOR STRUCTURES AND METHODS OF FABRICATING STRAIN COMPENSATED SEMICONDUCTOR STRUCTURES

Applicant:
Cree, Inc.

Relevant legal provisions:
EPC 1973 Art. 56
RPBA Art. 12(4)
RPBA 2020 Art. 13(2), 25(1), 25(2)

Keyword:
Inventive step - main request, first auxiliary request (no)
Late-filed second auxiliary request - admitted (no)
First and second auxiliary requests filed with the grounds of appeal - admitted (no)

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Case Number: T 1983/17 - 3.4.03

DECISION
of Technical Board of Appeal 3.4.03
of 7 September 2021

Appellant:
(Applicant)

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Representative:

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Decision under appeal:

Decision of the Examining Division of the European Patent Office posted on 27 March 2017 refusing European patent application No. 03784733.2 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman G. Eliasson
Members: M. Ley
T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 03 784 733.2 pursuant to Article 97(2) EPC.

II. The examining division decided that the subject-matter of claim 1 according to the main request lacked novelty (Article 52(1) EPC, Article 54(1) and (2) EPC 1973) over document D2 (WO 02/48434 A) and that the subject-matter of claim 16 according to the main request and of claim 1 according to an auxiliary request lacked an inventive step (Article 56 EPC 1973) over D2 and the common general knowledge of the skilled person.

Additional comments regarding *inter alia* the dependent claims were made in a section not forming part of the contested decision.

III. In a communication pursuant to Article 15(1) RPBA 2020, the Board raised objections under Articles 123(2) EPC, 84 EPC 1973, 52(1) EPC, 54(1) and (2) EPC 1973 and 56 EPC 1973 against the set of claims according the main request filed with statement setting out the grounds of appeal. Moreover, the Board informed the appellant about its provisional opinion that the admission of the first and second auxiliary requests filed with the statement setting out the grounds of appeal was to be discussed during the oral proceedings.

IV. In a letter dated 27 July 2021, the appellant filed claims according to a first and second auxiliary requests.

V. During oral proceedings before the Board, the appellant requested that the decision be set aside and a European patent be granted on the basis of the requests on file in the following order :

1. main request filed with the statement setting out the grounds of appeal
2. first auxiliary request filed with the letter dated 27 July 2021,
3. second auxiliary request filed with the letter dated 27 July 2021,
4. first auxiliary request filed with the statement setting out the grounds of appeal
5. second auxiliary request filed with the statement setting out the grounds of appeal

VI. Claim 16 according to the main request has the following wording (labelling **(A)** to **(G)** added by the Board):

A method of fabricating a semiconductor structure with first and second layers on a substrate, the method comprising:
(A) *forming the first layer (20) comprising a first Group III-nitride semiconductor material on a substrate (12);*
(B) *the substrate having a first in-plane unstrained lattice constant,*
(C) *the step of forming the first layer comprises the steps of:*
(C1) *forming 3D islands of the first semiconductor material on the substrate; and*
(C2) *growing the first semiconductor material such that the first semiconductor material coalesces in regions between the 3D islands; and*

(D) *forming the second layer (24) comprising a second Group III-nitride semiconductor material on the first layer;*
(E) *wherein the first layer has a second in-plane unstrained lattice constant that is mismatched with the first in-plane unstrained lattice constant of the substrate,*
(F) *the second layer is formed to have a third in-plane unstrained lattice constant that is different from the first in-plane unstrained lattice constant*
(G) *and the first layer is formed to have an in-plane strained lattice constant that is substantially matched to the third in-plane unstrained lattice constant of the second layer.*

Claim 1 according to the first auxiliary request filed with the letter dated 27 July 2021 has the following wording (labelling **(A')** to **(H)** added by the Board):

A method of fabricating a semiconductor structure with a first layer (20) and a second layer (24) on a substrate (12), the method comprising:
(A') *forming the first layer (20) directly on the substrate (12), the first layer comprising a first Group III-nitride semiconductor material,*
(B) *the substrate having a first in-plane unstrained lattice constant; and*
(D) *forming the second layer (24) comprising a second Group III-nitride semiconductor material on the first layer (20);*
(E') *wherein the first Group III-nitride semiconductor material of the first layer (20) has a second in-plane unstrained lattice constant that is mismatched with the first in-plane unstrained lattice constant;*
(C) *wherein the step of forming the first layer comprises the steps of:*

(C1) *forming 3D islands of the first semiconductor material on the substrate; and*
(C2) *growing the first semiconductor material such that the first semiconductor material coalesces in regions between the 3D islands,*
(H) *wherein the second in-plane unstrained lattice constant is sufficiently mismatched with the first in-plane unstrained lattice constant that the first layer (20) does not take on the lattice constant of the substrate but is strained such that the second in-plane unstrained lattice constant of the first Group III-nitride semiconductor material of the first layer (20) differs from a strained in-plane lattice constant of the first layer (20); wherein*
(F') *the second Group III-nitride semiconductor material of the second layer (24) has a third in-plane unstrained lattice constant that is different from the first in-plane unstrained lattice constant; and*
(G') *wherein the composition and/or growth conditions of the first layer (20) are selected to provide the first layer having the strained in-plane lattice constant that differs by less than 0.5% from the third in-plane unstrained lattice constant of the second layer (24).*

Claim 1 according to the second auxiliary request filed with the letter dated 27 July 2021 has the following wording:

A method of fabricating a semiconductor structure with a first layer (20) and a second layer (24) on a silicon carbide (SiC) substrate (12), the method comprising:
forming the first layer (20) directly on the substrate (12),
the first layer comprising a first Group III-nitride semiconductor material,

the SiC substrate having a first in-plane unstrained lattice constant,
wherein the step of forming the first layer comprises the steps of:
forming 3D islands of the first semiconductor material on the substrate; and
growing the first semiconductor material such that the first semiconductor material coalesces in regions between the 3D islands;
forming the second layer (24) comprising a second Group III-nitride semiconductor material on the first layer;
wherein the first Group III-nitride semiconductor material of the first layer (20) has a second in-plane unstrained lattice constant that is mismatched with the first in-plane unstrained lattice constant;
wherein the second Group III-nitride semiconductor material of the second layer (24) has a third in-plane unstrained lattice constant that is different from the first in-plane unstrained lattice constant;
wherein the step of forming a first layer (24) comprises forming a first layer so as to be strained at a growth temperature and strained when cooled from the growth temperature, wherein the amount of strain at the growth temperature compensates for the amount of strain induced in the first layer when cooled from the growth temperature to provide a desired in-plane strained lattice constant; and
wherein the first layer is formed to have an in-plane strained lattice constant that differs by less than 0.5% from the third in-plane unstrained lattice constant of the second layer (24).

Claim 14 according to the first auxiliary request filed with the statement setting out the grounds of appeal has the following wording:

A method of fabricating a semiconductor structure the method comprising:
providing a substrate (12) having a first in-plane unstrained lattice constant;
forming a strained first layer (20) disposed on and to adjacent the substrate (12),
the first layer comprising a first Group III-nitride semiconductor material
wherein forming the first layer comprises the steps of:
forming 3D islands of the first semiconductor material on the substrate; and
growing the first semiconductor material such that the first semiconductor material coalesces in regions between the 3D islands; and
forming a substantially unstrained second layer (24) on the first layer, the second layer comprising a second Group III-nitride semiconductor material;
wherein the first layer (20) has a second in-plane unstrained lattice constant that is mismatched with the first in-plane unstrained lattice constant of the substrate(12),
the second layer (24) is formed having a third in-plane unstrained lattice constant that is different from the first in-plane unstrained lattice constant, and
the first layer (20) is formed to have an in-plane strained lattice constant that differs compared to the third in-plane unstrained lattice constant of the second layer (24) by less than 1%.

Claim 1 according to the second auxiliary request filed with the statement setting out the grounds of appeal has the following wording:

A method of fabricating a semiconductor structure,
the method comprising:

providing a substrate (12) having a first in-plane unstrained lattice constant;
forming a strained first layer (20) disposed on and adjacent the substrate (12),
the first layer comprising a first Group III-nitride semiconductor material on a substrate (12)
the step of forming the second layer comprising the steps of:
forming 3D islands of the first semiconductor material on the substrate; and
growing the first semiconductor material such that the first semiconductor material coalesces in regions between the 3D islands; and
forming a substantially unstrained second layer (24) on the first layer (20),
the second layer comprising a second Group III-nitride semiconductor material;
wherein the first layer (20) has a second in-plane unstrained lattice constant that is mismatched with the first in-plane unstrained lattice constant of the substrate (12),
the second layer (24) is formed having a third in-plane unstrained lattice constant that is different from the first in-plane unstrained lattice constant of the substrate (12),
and the first layer (20) is formed to have an in-plane strained lattice constant that differs compared to the third in-plane unstrained lattice constant of the second layer(24) by less than 1%; and
wherein the step of forming the first layer (20) comprises forming a first layer (20) that is configured to provide a second layer that is strained at a growth temperature and substantially unstrained at a second temperature, different from the growth temperature.

VII. The appellant's arguments may be summarized as follows:

(a) Inventive step of the subject-matter of method claim 16 according to the main request

D2 disclosed a compositionally graded transition layer formed between a silicon substrate and a GaN layer, see page 6, lines 14 to 21, example 1, as a mechanism for relieving stress in a device layer (i.e. a second layer).

D2 did not disclose forming the transition layer 12 by 3D coalesced islands of a semiconductor material according to features **(C1)** and **(C2)**. 3D island growth (i.e. a Vollmer-Weber growth mode) was a known technique for epitaxial growth of thin films and resulted in rough films, wherein D2 mentioned MOCVD, MBE or hybride vapour phase epitaxy growth. When using the growth method according to **(C1)** and **(C2)**, atoms in the film were "more strongly bound to each other during growth than to the substrate surface", which allowed "growth of layers on a substrate with large lattice mismatch".

D2 did not disclose feature **(G)**. The example of page 6, lines 14 to 21 in D2 required that a composition of the graded transition layer at the front surface (adjoining the GaN layer 16) was GaN, so that the transition layer presumably had the unstrained lattice constant of GaN. Graded layer common in the art were grown to have a gradually changing composition so as to gradually transition from a material having the same or similar lattice constant as the substrate to a material having the same or similar lattice constant as the device layer. Increments in the change of composition were chosen so that strain in each sublayer was minimised.

The first and second layers were comprised of a respective first and second Group III-nitride semiconductor material "having uniform composition". The wording of claim 1 excluded that the first layer was a multilayer and/or had a graded composition or was composed of a plurality of (sub-)layers of different materials. Intervening layers between the first and second layer were not excluded. A selected portion of a graded layer did not correspond to the first layer according to the main request.

In summary, the appellant contested that document D2 disclosed a first layer in a strained state according to feature **(G)** and formed by steps **(C1)** and **(C2)**.

The appellant argued that the invention solved the problem of "how to provide a semiconductor structure with reduced defects at a second Group III nitride layer" and that this problem was solved by providing a strained first layer according to the distinguishing features. As a result of feature **(G)**, the second layer according to the invention was "substantially unstrained" so that homogeneous upper device layers with fewer dislocations or defects could be prepared thereon. Dislocations could however occur in the first layer.

The skilled person would have no motivation to include a first layer according to feature **(G)** in the structure known from D2. None of the documents cited by the examining division would suggest to do so.

The appellant also pointed out that the presented invention aimed at providing a "quasi-substrate" used to receive further device layers, wherein the substrate could possibly be removed.

(b) Inventive step of the subject-matter of claim 1 according to the first auxiliary request filed with the letter dated 27 July 2021

In addition to the arguments provided for the main request, the appellant added that the first layer according to claim 1 was formed as one single layer having a uniform composition and a uniform strained in-plane lattice constant differing by less than 0.5 % from the unstrained in-plane lattice constant of the second layer throughout its entire thickness; the first layer being formed directly on the substrate.

The wording of claim 1 thus excluded the compositionally graded transition layer 12 of D2 (as well as the embodiment of page 12, lines 18 to 26 of the application). The AlN layer at the interface 18 of figure 1 in D2 could not be considered as first layer in the sense of claim 1, as it would not be produced in accordance with feature **(G')**. The skilled person would not replace the graded transition layer 12 of D2 by a first layer according to claim 1.

(c) Admission of the second auxiliary request filed with the letter dated 27 July 2021

In its letter dated 27 July 2021, the appellant stated that this second auxiliary request defined essentially the same invention although with different formulations of the claims and was prima facie clearly allowable. Furthermore, the request was filed in response to the Board's objections, in particular the added-matter and clarity objections, and did not raise any new issues.

(d) Admission of the first and second auxiliary requests filed with the statement setting out the ground of appeal

In section "1. Admissibility" of the statement setting out the grounds of appeal, the appellant stated that the amendments made to the first and second auxiliary requests addressed the deficiencies noted in the contested decision and, in particular, the objection to a lack of novelty.

Reasons for the Decision

1. The appeal is admissible.

2. The present invention relates to a method of providing semiconductor structures with a Group III-nitride semiconductor layer (e.g. a GaN layer) on a semiconductor substrate (made of e.g. SiC or sapphire), wherein the semiconductor layer is made of a material having an in-plane unstrained lattice constant different from the one of the substrate. The semiconductor layer can be used to produce semiconductor devices (e.g. LEDs, FETs) or can be used as a seed crystal for growing further semiconductor layers, see page 6, line 25 to 29 or page 12, lines 14 to 17 of the application.

Due to the difference in lattice constants, the semiconductor layer grown on the substrate may be strained. If the level of strain exceeds a threshold, the semiconductor material cracks which renders it unacceptable for use in a semiconductor device, see page 1, lines 10 to 22 of the application.

The invention solves this well-known problem by providing an intermediate layer between the substrate and the semiconductor layer. The intermediate layer is made of a Group-III nitride semiconductor material having an unstrained in-plane lattice constant different from the one of the substrate. Said intermediate layer has an in-plane strained lattice constant which substantially matches the in-plane unstrained lattice constant of the semiconductor layer. As a result, stress in the semiconductor layer is reduced and cracking is avoided, see page 12, lines 4 to 14 of the application.

3. Main request

3.1 In the Board's view, D2 discloses a semiconductor structure (figure 1), comprising a substrate (14) having a first in-plane unstrained lattice constant (page 2, line 6, page 4, line 28, "silicon substrate", lattice constant for relaxed (100) silicon = 5.43 Å, page 11, lines 1 to 21); a first layer (transition layer 12) of a first semiconductor material (page 5, line 11 to page 9, line 6, $Al_xGa_{1-x}N$ for example) on the substrate (14); and a second layer (16) comprising a second semiconductor material (GaN, page 9, line 7 to page 10, line 32); wherein the first layer (12) is located between the substrate (14) and the second layer (16), see figure 1. When fabricating the semiconductor structure, the first and second layers 12, 16 are formed in that order on substrate 14, see e.g. page 3, lines 3 to 6.

In a relaxed state, the semiconductor materials used for transition layer 12 in D2 (e.g. $Al_xGa_{1-x}N$ having an unstrained in-plane lattice constant between 3.11 Å if x = 1 and 3.19 Å if x = 0) have an in-plane lattice constant different or mismatched from the one of the relaxed silicon substrate 14 (5.43 Å).

Moreover, in a relaxed state, the material of the second layer (16) in D2 (i.e. GaN) has a lattice constant (3.19 Å for GaN) that is different or mismatched from the one of the silicon substrate.

Thus D2 discloses features **(A)**, **(B)**, **(D)**, **(E)** and **(F)**.

3.2 Feature **(G)** requires that the first layer is formed to have an in-plane strained lattice constant that is substantially matched to the third in-plane unstrained lattice constant of the second layer.

The Board takes the view that this wording does not imply that the entire first layer is strained with the same in-plane strained lattice constant (that is substantially matched to the unstrained in-plane lattice constant of the second layer) and/or with a homogenous or uniform composition throughout its entire thickness. Claim 16 merely requires a first layer comprising a sub-part having the strained lattice constant according to feature **(G)**, said sub-part being necessarily close to the second layer in order to achieve the desired effect of reducing stress in the second layer. A first layer including several sub-layers or a graded composition is not excluded, see also page 9, lines 23 to 25, page 11, lines 2 to 5 of the application.

D2 discloses a number of possible arrangements for the transition layer 12 (page 6, line 11 to page 9, line 6, figures 2A to 2I, 3A, 3B, 4A, 4B). The transition layer is provided in D2 to "lower stresses in the gallium nitride material layer which can result from differences in thermal expansion rates between the gallium nitride material and the substrate", see D2, page 2, lines 8 to 11, page 4, lines 29 to 32, page 5, lines 15 to 17, page 9, lines 21 to 23. In one example of D2, the transition layer 12 is a compositionally graded $Al_xGa_{1-x}N$ layer, see page 5, lines 18 to page 6, line 8, which corresponds to a preferred embodiment of the present application, see e.g. original claims 22 - 24. In this type of layer, as it is known to the skilled person from its common general knowledge, the lattice constant linearly varies from 3.11 Å if x = 1 and 3.19 Å if x = 0. As pointed out by the appellant, such graded semiconductor layers are known in the art and typically have a gradually changing composition so as to gradually transition from a material having the same or similar lattice constant as the substrate to a material having the same or similar lattice constant as the device layer, see also D2, page 6, lines 9 to 27.

Close to the interface 18 of substrate 14 and transition layer 12, the latter must be strained in view of the difference in lattice constant between silicon and AlN, as it is normally the case when a layer of a Group III-nitride semiconductor material is formed on a silicon substrate due to the high lattice constant mismatch.

Furthermore, as D2 states that the transition layer is to "lower stresses in the gallium nitride material layer" 16, see e.g. page 5, lines 29 to 30, a skilled person would understand that at the interface 20 in figure 1 of D2, the second layer made of GaN is "substantially unstrained", but not necessarily completely relaxed. Hence, the transition layer is also under strain close to the interface 20 with the second layer/gallium nitride material layer 16. It can thus be said that the transition layer 12 in D2 is a strained layer.

D2 mentions that close to said interface 20, the transition layer 12 is composed of $Al_xGa_{1-x}N$, with x less than 0.2, see page 6, line 11 to 13, in which case the in-plane lattice constant would be smaller than 0.2 * 3.11 + 0.8 * 3.19 = 3.17 Å. As the unstrained in-plane lattice constant of GaN layer 16 is 3.19 Å and as the transition layer 12 provides the same effect as the first layer according to the invention - namely to reduce stress in the second layer -, transition layer 12 is not only strained, but has at least in a region close to the interface 20 a strained in-plane lattice constant that "is substantially matched to the third in-plane unstrained lattice constant of the second layer".

Hence, feature **(G)** is also disclosed in D2.

3.3 In D2, the structure shown in figure 1 of D2 is used as "quasi-substrate" for receiving further semiconductor layers to provide a semiconductor device, see figures 7 to 9, page 14, line 21 to page 15, line 29. The Board notes that nothing in method claim 16 suggests that the substrate is removed at any stage of the process.

3.4 The Board agrees with the examining division and the appellant that D2 does not disclose the mode of growing transition layer 12. D2 does not disclose forming the first layer as defined by features **(C1)** and **(C2)**.

In view of the considerations made in sections 3.1 to 3.3 above, the Board judges that the claimed method differs from the disclosure of D2 only by said two features.

3.5 The alleged technical problem (see section VII.(a), seventh paragraph) is already solved in D2 in view of page 2, lines 8 to 11, page 4, lines 29 to 32, which implies that a substantially unstrained GaN layer with reduced defects is obtained. The reason is that D2 discloses a transition layer 12 according to claim 16 and, in particular, in accordance with feature **(G)**.

The only difference between D2 and the claimed method are steps **(C1)** and **(C2)**. D2 discloses several deposition techniques for forming the semiconductor layers 14 and 20, see page 12, lines 26 to 31. Although more details were given for MOCVD (see page 13, line 1 to page 14, line 20), said passage on page 12 makes it clear that any other suitable technique known in the art may be utilized. D2 is silent about the growth mode used in the method.

The objective technical problem would therefore be how to find an adequate growth mode for the transition layer 12 in D2.

There are three primary modes by which thin films grow epitaxially at a crystal surface of a substrate:
- Frank–Van der Merwe growth or 'layer-by-layer growth' is considered an ideal growth model, requiring perfect

lattice matching between the substrate and the layer growing onto it.
- In Volmer-Weber growth, adatom-adatom interactions are stronger than those of the adatom with the surface, leading to the formation of three-dimensional adatom clusters or islands, see also the appellant's explanations in the statement setting out the grounds of appeal, page 4, last paragraph.
- Stranski-Krastanov growth is an intermediary process characterized by both 2D layer and 3D island growth.

The skilled person wishing to solve the objective technical problem would have to select between these three possibilities.

In view of lattice mismatch between substrate 14 and transition layer 12 in D2, Frank-Van der Merwe growth is not possible. The skilled person would thus have to select a growth mode involving three dimensional islands. The Board is convinced that it would be obvious for the skilled person to perform the growth of $Al_xGa_{1-x}N$ transition layer 12 by the well-known Vollmer-Weber growth mode. It would have to choose the deposition conditions of D2 such that steps (C1) and (C2) are performed to produce transition layer 12.

Hence, the subject-matter of claim 16 of the main request lacks an inventive step (Article 56 EPC 1973) in view of D2 and the common general knowledge of the skilled person.

4. First auxiliary request filed with the letter dated 27 July 2021

4.1 The Board accepts that the amendments made to claim 1 of the first auxiliary request filed with the letter dated 27 July 2021 (including the deletion of all device claims) is a response to the objections under Article 123(2) EPC and (84) EPC 1973 raised by the Board against the claims of the main request. This request is thus admitted into the appeal procedure (Article 13(2) RPBA 2020 in combination with Article 25(1) RPBA 2020).

4.2 The Board notes that amended features **(E')** and **(F')** are disclosed in D2 for reasons already given in section 3.1 above.

As transition layer 12 (i.e. the "first layer") is formed directly on the substrate 14, D2 also discloses amended feature **(A')**.

Feature **(H)** defines not more than the fact that the first layer is under strain as a result of the difference in lattice constant of the materials of the substrate and the first layer. For the reasons given in section 3.1 above, this feature is also disclosed in D2 in view of the large difference in lattice constant (5.43 Å for Si and 3.11 Å for AlN). This has not been contested by the appellant.

4.3 With respect to amended feature **(G')**, the Board is of the view that the appellant's reading of claim 1 (see section VII.(b) above) is not supported by or disclosed in the application as originally filed.

According to the appellant, the first layer would have a strained in-plane lattice constant differing by less than 0.5 % from the unstrained in-plane lattice constant of the second layer throughout its entire thickness. This would mean that even at the direct interface between the substrate and the first layer the first layer has a lattice constant which "substantially matches" the lattice constant of the second layer, i.e. differs therefrom by less than 0.5%. This type of layer is not disclosed in the application as originally filed.

From page 1, line 25 to page 2, line 22, from page 2, line 29 to page 3, line 4 in combination with page 3, lines 10 to 15 or from page 6, line 25 to page 7, line 15 of the application or from claims 25, 26, 32 to 34, claims 44 and 47 to 49, a skilled person would understand that the claimed lattice mismatch of less than 0.5 % concerns the surface of the mismatch layer (first layer) facing the device match layer (second layer) to reduce stress in the device match layer and obtain a higher crystalline quality with fewer defects. From the application as a whole the skilled person would not derive that the same lattice constant mismatch might be present close to the substrate's surface. Quite the contrary, the skilled person would expect that the lattice constant in that part of the mismatch layer is closer to the substrate's unstrained lattice constant.

The Board thus takes the view that claim 1 merely requires a first layer comprising a sub-part having the strained lattice constant according to feature **(G')**, said sub-part being necessarily close to the second layer in order to achieve the desired effect of reducing stress in the second layer.
In view of the considerations of section 3.2 above, D2 thus discloses that the composition and/or growth conditions of the first layer (12) are selected to provide the first layer (12) having the strained in-plane lattice constant that differs from the third in-

plane unstrained lattice constant of the second layer (24). D2 does not disclose the claimed value of 0.5 %.

The subject-matter of claim 1 of the first auxiliary request filed with letter dated 27 July 2021 differs therefore from D2 by features **(C1)** and **(C2)** and by the specific value of "less than 0.5%".

The Board could not identify any synergistic effect between the distinguishing features either in the application as originally filed or in the appellant's explanations. The inventive merit of these features can therefore be assessed separately.

Features **(C1)** and **(C2)** are obvious for the reasons given for the main request, see section 3.5 above.

With respect to the value of "less than 0.5%", D2 teaches that a GaN layer 16 of better crystalline quality can be manufactured as a result of the reduced internal stress provided by the transition layer 12, see e.g. page 5, lines 3 to 5; said stress resulting from differences in lattice constants and thermal expansion coefficients, see page D2, page 1, lines 19 to 31. A high gallium concentration at the interface 20 (see figure 1) is particularly effective in relieving internal stress, see page 5, lines 27 to 30. According to D2, page 6, lines 9 to 29, a high gallium concentration is obtained e.g. by using $Al_xGa_{1-x}N$ with $0 \leq x \leq 0.2$ as the material of the transition layer 12 close to the interface 20. The skilled person using its common general knowledge would understand that it is thus advantageous to have a lowest possible difference in lattice constant between transition layer 12 and GaN layer 16 at the interface 20. The Board is of the view that a difference of 0.5% or less is obvious for the skilled person wishing to minimize the lattice mismatch at the interface 20. An inventive step on the basis of the value of "less than 0.5%" cannot be acknowledged.

4.4 Hence, the subject-matter of claim 1 according to the first auxiliary request filed with the letter dated 27 July 2021 does not involve an inventive step (Article 56 EPC 1973) in view of D2 and the common knowledge of the skilled person.

5. Admission of the second auxiliary request filed with letter dated 27 July 2021

According to Article 13(2) RPBA 2020 in combination with Article 25(1) RPBA 2020, any amendment to a party's appeal case made after notification of a summons to oral proceedings shall, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned.

The second auxiliary request filed with letter dated 27 July 2021 was filed after notification of the summons to oral proceedings.

The Board admitted the first auxiliary requests filed with the same letter, because the amendments made only address the objections raised by the Board in its communication pursuant to Article 15(1) RPBA 2020, see section 4.1 above.

However, the inclusion of the features "*wherein the step of forming a first layer (24) comprises forming a first layer so as to be strained at a growth temperature and strained when cooled from the growth temperature, wherein the amount of strain at the growth* *temperature compensates for the amount of strain induced in the first layer when cooled from the growth temperature to provide a desired in-plane strained lattice constant"* in claim 1 of the second auxiliary request introduce new aspects not discussed before the examining division, in the statements setting out the grounds of appeal or in the Board's communication.

Moreover, the Board has doubts whether the passage indicated by the appellant (page 9, last line to page 10, line 6 of the application as originally filed) provides a basis for said feature. The Board also notes that claims 60 and 61 as originally filed do not specifically concern a SiC substrate or a first layer with feature **(G')**. Finally, the Board questions the clarity of the expression "*the amount of strain at the growth temperature compensates for the amount of strain induced in the first layer when cooled from the growth temperature".*

In other words, claim 1 does not merely define the same invention as the higher ranking requests using a different wording and the amendments made do raise new issues to be discussed for the first time during oral proceedings before the Board. The reasons brought forward by the appellant (see section VII.(c) above) do not justify "exception circumstances" in the sense of Article 13(2) RPBA 2020.

Therefore, the Board did not admit the second auxiliary request filed with letter dated 27 July 2021 into the proceedings.

6. Admission of the first and second auxiliary requests filed with the statement setting out the grounds of appeal

According to the statement of grounds of appeal, paragraph bridging pages 6 and 7, the amendments to the independent claims of both requests were made as a reply to the "Examining Division's annexed comments". As the examining division's issues were already raised in the summons to oral proceedings (see e.g. points 3 and 4, in particular), the appellant should have filed both auxiliary requests during the examination procedure. For this reason, the Board does not admit them into the proceedings under Article 12(4) RPBA 2007 in combination with Article 25(2) RPBA 2020.

Regarding the first auxiliary request, the Board observes that the scope of claim 14 is broader than the scope of claim 1 of the higher ranking first auxiliary request filed with the letter dated 27 July 2021 and thus for the same reasons does not involve an inventive step (Article 56 EPC).

Claim 1 of the second auxiliary request corresponds to method claim 14 of the first auxiliary request, wherein the feature "wherein the step of forming the first layer (20) comprises forming a first layer (20) that is configured to provide a second layer that is strained at a growth temperature and substantially unstrained at a second temperature, different from the growth temperature." has been added. As the application as originally filed is silent about how the first layer has to be "configured" to obtain the claimed effect, the Board is of the view that this feature would raise new issues to be discussed for the first time before the Board.

7. As no allowable request is on file, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

Beschwerdekammern des Europäischen Patentamts
Boards of Appeal of the European Patent Office
Chambres de recours de l'Office européen des brevets

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated