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Title of invention:
Metallization structure for high power microelectronic devices

Applicant:
Cree, Inc.

Relevant legal provisions:
EPC Art. 56
RPBA Art. 12(2), 12(4)
RPBA 2020 Art. 25(2)

Keyword:
Inventive step - main request, second auxiliary request- (no)
First auxiliary request - admitted (no)

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Case Number: T 2154/17 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 6 October 2021

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	FRKelly 27 Clyde Road Dublin D04 F838 (IE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 10 April 2017 refusing European patent application No. 08171317.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	S. Ward
Members:	M. Ley
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 08 171 317.4 pursuant to Article 97(2) EPC.

The following documents were cited:

D1 DE 10 2004 036142 A1
D2 EP 1 744 374 A
D5 US 5 286 676 A
D6 US 5 518 805 A

The examining division decided that claim 1 according to a main request and to a first auxiliary request lacked clarity (Article 84 EPC) and that the subject-matter of claim 1 according to the first auxiliary request lacked an inventive step (Article 56 EPC). The examining division did not admit late-filed second auxiliary request into the proceedings under Rule 137(3) EPC, because it was *prima facie* not allowable under Articles 123(2) and 56 EPC.

II. The appellant initially requested that the impugned decision be set aside and a European patent be granted on the basis of a main request or of a first auxiliary request filed with the statement setting out the grounds of appeal. In the alternative, the appellant requested that the application be remitted to the examining division for further examination. Oral proceedings were requested in the event that the Board was minded to take any decision adverse to the appellant.

III. In a communication pursuant to Article 15(1) RPBA 2020, the Board informed the appellant about its preliminary view that claims 1, 11, 12 and 16 according to the main request did not comply with Article 123(2) EPC, that claim 1 according to the main request lacked clarity (Article 84 EPC) and that its subject matter was either not new (Articles 52(1), 54(1) and (2) EPC) or did not involve an inventive step (Article 56 EPC). The first auxiliary request should not be taken into account in accordance with Article 12(4) RPBA 2007 in combination with Article 25(2) RPBA 2020.

IV. With a letter dated 26 August 2021, the appellant filed an amended main request to replace the main request hitherto on file and a set of claims according to a second auxiliary request.

V. The appellant informed the Board with a letter dated 24 September 2021 that it would not attend the oral proceedings. The oral proceedings were cancelled.

VI. Claim 1 according to the main request has the following wording (Board's labelling **(a)** to **(l)**):

(a) *A power semiconductor device structure (10) comprising:*
(b) *a wide-bandgap semiconductor portion (12) selected from silicon carbide and Group III nitrides;*
(c) *an interconnect structure (11) to said wide-bandgap semiconductor portion,*
(d) *said interconnect structure including at least two high electrical conductivity layers (14) alternating with respective diffusion barrier layers (13)*
(e) *such that each high electrical conductivity layer is between two respective diffusion barrier layers;*

(f) *a first adhesion layer, wherein a lowermost of the diffusion barrier layers is directly on a surface of the first adhesion layer and*
(f1) *the first adhesion layer is between the lowermost of the diffusion barrier layers and a portion of the semiconductor device structure selected from said wide-bandgap semiconductor portion, an ohmic contact, a Schottky contact, and a dielectric layer;*
(g) *a second adhesion layer directly on a topmost of the diffusion barrier layers and*
(g1) ***the second adhesion layer is between the uppermost of the diffusion barrier layers and another portion of the semiconductor device structure selected from a dielectric, a polymer, and a metal,***
(h) *wherein the first and second adhesion layers are separate and distinct from the diffusion barrier layers;*
(i) *said diffusion barrier layers having a coefficient of thermal expansion different from and lower than the coefficient of thermal expansion of said high electrical conductivity layers; and*
(j) ***the difference in the respective coefficients of thermal expansions being large enough to constrain the expansion of said high conductivity layers but less than a difference that would create a strain between adjacent layers that would exceed the bond strength between the layers during use of the semiconductor structure,***
(k) ***wherein the high electrical conductivity layers have a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of said diffusion barrier layers by a factor of between 1.5 and 2 and***
(l) ***the interconnect structure has a thickness of between 0.1 and 10 µm.***

Claim 1 according to the first auxiliary request has features (a) to (e), (e1), (f'), (g'), (h) to (k) and (l'), wherein features (e1), (f'), (g') and (l') read:

(e1) *wherein a thickness of each of the high electrical conductivity layers is greater than a thickness of each of the diffusion barrier layers;*

(f') *a first adhesion layer, wherein a first of the diffusion barrier layers is directly on a surface of the first adhesion layer;*

(g') *a second adhesion layer directly on a second of the diffusion barrier layers,*

(l') ***the interconnect structure has a thickness of between 0.1 and 10 microns.***

Claim 1 according to the second auxiliary request corresponds to claim 1 of the main request, wherein the first and second adhesion layers are "separate from the interconnect structure".

VII. The appellant's arguments will be discussed below.

Reasons for the Decision

1. Procedural matters

1.1 In the statement of grounds of appeal, the appellant noted that the main request was rejected by the examining division only for clarity reasons, although section "III. Further comments" at the end of the contested decision indicated that claim 1 according to the main request lacked an inventive step. The appellant assumed "that the listing of claim 1 of the

Main Request as having prior art rejection in the last paragraph of the Decision to Refuse was an error".

In view of the section 1. of the Reasons for the Decision, the Board concurs with the appellant that the main request underlying the contested decision was formally refused for a lack of clarity alone and section III. of the contested decision concerns further comments not forming part of the decision. The Board is satisfied that the addition of features (k) and (l) as well as the arguments provided by the appellant on clarity sufficiently address the reasons that led to the refusal of the main request, although the appellant did not address the objections under Article 56 EPC raised against the first auxiliary request underlying the decision.

Hence, the appeal is admissible.

1.2 The appellant's declaration of non-attendance at the oral proceedings is considered by the Board as equivalent to a withdrawal of its request for oral proceedings (see Case Law of the Boards of Appeal of the European Patent Office, 9th Edition, 2019, III.C. 4.3.2).

Taking into account the appellant's arguments provided in its letter dated 26 August 2021, the Board concludes that the case is ready for decision without oral proceedings.

2. The invention concerns interconnect metal structures for semiconductor devices with three or more terminals that operate at relatively high power and include a wide-bandgap semiconductor portion selected from silicon carbide or group III-nitride semiconductors.

Examples of such semiconductor devices are insulated gate field effect transistors (see figure 2), high electron mobility transistors (figure 3) or metal-semiconductor field effect transistors (figure 5).

Because wider bandgap materials can operate at higher power than lower bandgap materials, the thermal stresses on interconnect metals are greater in wide bandgap material devices than they are in silicon-based or gallium arsenide-based devices, see paragraph [0010] of the application. For metal interconnect structures comprising a plurality metal layers, the thermal expansion stress tends to cause the layers to delaminate from one another due to differences in coefficients of thermal expansion, see paragraphs [0011] to [0014] of the application.

The invention suggests to avoid such undesired delamination by providing an interconnect structure including at least two diffusion barrier layers alternating with two respective high electrical conductivity layers. The diffusion barrier layers have a coefficient of thermal expansion different from and lower than the coefficient of thermal expansion of the high electrical conductivity layers. The difference in the respective coefficients of thermal expansions is large enough to constrain the expansion of the high conductivity layers but less than a difference that would create a strain between adjacent layers that would exceed the bond strength between the layers. According to paragraph [0030] of the application, this effect is achieved when the high electrical conductivity layers have a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of said diffusion barrier layers by a factor of between 1.5 and 2.

3. Main request

The Board accepts that the amendments made to the main request only addressed the objections under Articles 123(2) and 84 EPC raised by the Board for the first time in sections 4.2 and 4.3.2 of its communication. The main request is thus admitted into the proceedings.

3.1 Clarity - Article 84 EPC

3.1.1 The examining division held that "the scope of protection being sought" by feature (j) was "not clearly defined", because claim 1 placed "no restrictions concerning the conditions of use" under which the conditions of feature (j) should be met, see the contested decision, section 2. of the Reasons for the Decision. As examples of device operating conditions, the examining division named power, temperature, duration. Furthermore, the addition of features (k) and (l) were not sufficient to clarify claim 1, see the contested decision, section 3.1, relating to the clarity of the first auxiliary request. The examining division stated that the "thicknesses of the respective layers" were "essential for constraining the expansion of the high electrical conductivity layer while keeping strain below the bond strength". It would be unlikely that very thin diffusion barrier layers would be capable of constraining the expansion of very thick high electrical conductivity layers.

3.1.2 The appellant argued that paragraph [0036] made it clear that very thin, e.g. 50 nm thin, diffusion barrier layers were capable of constraining very thick, e.g. 1500 nm thick, high electrical conductivity layers. Furthermore, the appellant argued that the skilled person would "readily appreciate" that in view

of features (i) to (l), there was an "inherent limit on the layer thicknesses".

3.1.3 With respect to feature (j) as such, the Board is of the opinion that claim 1 defines the difference in coefficients of thermal expansion so that a certain result is achieved, namely to constrain the expansion of said high conductivity layers without creating a strain between adjacent layers that would exceed the bond strength between the layers during use of the semiconductor structure. In other words, feature (j) merely states that the problem to be solved described in paragraphs [0010] to [0014] of the application as originally filed, namely an undesired delamination of the layers of the interconnect structure, would not occur by an adequate choice of the CTEs.

In view of paragraphs [0031], [0032] and [0036], the Board is satisfied that the claimed factor of 1.5 and 2 between the CTEs for an 10 to 1000 nm thick interconnect structure allows to constrain the expansion of said high conductivity layers, even for a diffusion barrier layer being "very thin" compared to the respective high electrical conductivity layers, without creating "a strain between adjacent layers that would exceed the bond strength between the layers during use of the semiconductor structure". The Board understands by "use" the normal use of the semiconductor structure.

Hence, contrary to the findings of the examining division, the Board is satisfied that features (j) to (l) do not render claim 1 unclear and that the effect of (j) is automatically obtained when an interconnect structure according to features (c), (d) and (i) also includes features (k) and (l), in accordance with

paragraphs [0017], [0031] and [0032] of the application.

3.2 Inventive step - Article 56 EPC

3.2.1 Interpretation of features (c) to (e)

In its communication pursuant to Article 15(1) RPBA 2020, section 4.5, the Board noted that the wording of claim 1 does not exclude an interconnect structure including the first and second adhesion layers, i.e. that the adhesion layers are parts of the interconnect structure. As a consequence, D1 might possibly be novelty destroying for claim 1 according to the main request filed with the statement setting out the grounds of appeal.

In its letter dated 26 August 2021, page 3, last three paragraphs, the appellant argued that the wording of the claim according to the main request specified that the first and second adhesion layers were not "within the interconnect structure".

The Board has doubts whether the appellant's reading of claim 1 is accurate, but gives the appellant the benefit of the doubt and makes the assumption that the first and second adhesion layers are not part of the interconnect structure so that the lowermost and uppermost aluminum layers in D1 cannot be considered as adhesion layers. The Board considers it likely that the examining division made the same assumption when deciding on inventive step in the context of the first auxiliary request underlying the decision, see sections 3.2 of the Reasons for the Decision.

Hence, under the above assumption, claim 1 defines a semiconductor device structure according to figure 1. The interconnect structure is a stack of at least two high electrical conductive layers (14) alternating with respective diffusion barrier layers (13) such that each high electrical conductivity layer (of the stack) is between two respective diffusion barrier layers; the lowermost diffusion barrier layer 13 being directly on the first adhesion layer 15 and the second adhesion layer 15 being directly on the uppermost diffusion barrier layer 13.

3.2.2 Document D1

Document D1 discloses an interconnect structure 40 for a semiconductor portion 10, which has a reduced electromigration, see D1, paragraph [0009] and includes a stack of alternating aluminium layers and diffusion barrier layers. In the example of figure 2 and paragraph [0025], the structure comprises three aluminum layers 11, 12 and 13 and between them two diffusion barrier layers 21, 22. The last sentence of paragraph [0025] reads "Die Metallisierung 40 kann in entsprechender Weise beliebig erweitert bzw. aufgebaut werden, indem auf der dem Halbleitersubstrat 1 abgewandten Vorderseite der dritten Metallisierungs-schicht 13 abwechselnd eine Barriereschicht und eine Metallisierungsschicht erzeugt werden." This makes it clear that the structure shown in figure 2 can additionally comprise a third diffusion barrier and a fourth aluminum layer. In other words, D1 discloses an interconnect structure comprising the following stack: first Al layer 11/first diffusion barrier layer 21/ second Al layer 12/second diffusion barrier layer 22/ third Al layer 13/third diffusion barrier layer/fourth Al layer.

D1 thus discloses an interconnect according to features (c) and (d). However, in view of section 3.2.1 above, D1 does not disclose feature (e), as only the second and third aluminium layers 12, 13 are each between two respective diffusion barrier layers, namely between diffusion barrier layers 21 and 22 and between diffusion barrier layer 22 and the third diffusion barrier layer (not shown in figure 2), respectively. Aluminium layer 11 and the fourth aluminium layer (not shown) do not meet the condition according to feature (e).

Hence, in the wording of claim 1 according to the main request, D1 discloses (see figures 2, 3 and 5 and the description associated thereto):
a power semiconductor device structure (figure 3, paragraph [0030], power semiconductor device, "Leistungshalbleiterbauelement") comprising:
a wide-bandgap semiconductor portion (1) selected from silicon carbide and Group III nitrides ([0021], "Siliziumkarbid");
an interconnect structure (40) to said wide-bandgap semiconductor portion (1),
said interconnect structure (40) including at least two high electrical conductivity layers (figure 2, 12, 13, [0022], "Aluminium", [0024]) alternating with respective diffusion barrier layers ([0022], [0025], "Barriereschicht", "Nickel", "Titan", figure 2, 21, 22, third diffusion barrier layer not shown in figure 2) such that each <u>of said two</u> high electrical conductivity layers is between two respective diffusion barrier layers (the two Al layers 12, 13 and the diffusion barrier layers 21, 22 plus the third diffusion barrier layer not shown in figure 2 fulfil this condition);
~~a first adhesion layer, wherein a lowermost of the diffusion barrier layers is directly on a surface of~~

~~the first adhesion layer a~~nd ~~the first adhesion layer is between the lowermost of the diffusion barrier the layers and~~ the interconnect structure (40) is on a portion of the semiconductor device structure (1) selected from said wide-bandgap semiconductor portion, an ohmic contact, a Schottky contact, and a dielectric layer (figures 2 and 5);
a second adhesion layer ([0024], "Oxidschicht als Haftvermittler") directly on ~~a topmost of the diffusion barrier layers~~ the interconnect structure (40) and the second adhesion layer is between the ~~uppermost of the diffusion barrier layers~~ interconnect structure (40) and another portion of the semiconductor device structure selected from a dielectric, a polymer, and a metal ([0024], nitride layer "Nitridschicht"),
wherein the ~~first and~~ second adhesion layer~~s are~~ is separate and distinct from the diffusion barrier layers;
said diffusion barrier layers (21, 22) having a coefficient of thermal expansion different from and lower than the coefficient of thermal expansion of said high electrical conductivity layers (Al: 23 x 10^{-6} K^{-1}, Ni: 13.4 x 10^{-6} K^{-1}); and
the difference in the respective coefficients of thermal expansions being large enough to constrain the expansion of said high conductivity layers but less than a difference that would create a strain between adjacent layers that would exceed the bond strength between the layers during use of the semiconductor structure (implicit, in view of the CTEs and the total thickness used),
wherein the high electrical conductivity layers have a coefficient of thermal expansion that is greater than a coefficient of thermal expansion of said diffusion barrier layers by a factor of between 1.5 and 2 (CTE_{Al} = 1.7 x $CTE_{Ni)}$ and

the interconnect structure has a thickness of between 0.1 and 10 µm (D1, [0028]: 1 µm, 3 µm, 5 µm, 10 µm).

3.2.3 Distinguishing features

Under the assumption of section 3.2.1 above, the subject-matter of claim 1 thus differs from D1 in that:
(A) each high electrical conductivity layer is between two respective diffusion barrier layers;

(B) a first adhesion layer, wherein a lowermost of the diffusion barrier layers is directly on a surface of the first adhesion layer and the first adhesion layer is between the lowermost of the diffusion barrier layers and said portion of the semiconductor device structure selected from said wide-bandgap semiconductor portion, an ohmic contact, a Schottky contact, and a dielectric layer;

(C) the second adhesion layer is directly on a topmost of the diffusion barrier layers and the second adhesion layer is between the topmost/uppermost of the diffusion barrier layers and said another portion of the semiconductor device structure selected from a dielectric, a polymer, and a metal.

Distinguishing features (A) to (C) correspond to the differences (i) and (ii) identified by the examining division, see section 3.2.2 of the appealed decision.

3.2.4 Partial technical problems and obviousness

There is no indication in the application as originally filed or the appellant's written submissions that any synergistic effect exists between features (A) to (C).

It appears therefore appropriate to formulate a partial technical problem for each of the distinguishing features, as did the examining division.

(a) distinguishing feature (A)

In its letter dated 26 August 2021, page 4, fourth to sixth paragraphs, the appellant argued that the claimed structure addressed the problem of thermal expansion and that distinguishing feature (A) ensured that thermal expansion of each high electrical conductivity layer was constrained without causing delamination according to feature (j). None of the cited references recognized this problem or provided any type of solution for this problem. D1 was only concerned with positioning a barrier layer 21, 22 between pairs of metallization layers 11, 12, 13 to reduce migration between the metallization layers 11, 12, 13. D6 disclosed the exact same relationship where a barrier metal 56 was positioned between pairs of base metal sublayers 54. D6 might indicate that the alternating order of the barrier metals 56 and the base metal sublayers 54 might be reversed (see D6, col. 4, lines 61 to 64). However, D6 specifically indicated in the same passage at col. 4, line 66 through col. 5, line 3 and col. 5, lines 20 to 31 that "the important aspects of the present invention are that any layer of the base metal is less than the critical thickness and that any two adjacent layers of the base metal is separated by a barrier metal of some type." D1 and D6 failed to disclose distinguishing feature (A), which resulted in a greater number of diffusion barrier layers relative to a number of high electrical conductivity layers.

The Board is not convinced by the appellant's argumentation. According to paragraph [0017] of the

application and claim 1 as originally filed, the effect according to feature (j) is achieved by providing an "interconnect structure including at least two diffusion barrier layers alternating with two respective high electrical conductivity layers", wherein the diffusion barrier layers have a coefficient of thermal expansion different from and lower than the coefficient of thermal expansion of the high electrical conductivity layers. In other words, the problem of undesired delamination is solved by an interconnect structure having features (c), (d) and (i). As the structure known from D1 clearly has these three features, the objective technical problem solved by distinguishing feature (A) cannot be the one indicated by the appellant.

The fact that each high electrical conductivity layer is between two respective diffusion barrier layers implies that the lowermost and uppermost layers of the interconnect structure are diffusion barrier layers. The partial problem related to distinguishing feature (A) is to avoid undesired aluminium diffusion into the elements underlying and overlying the interconnect structure 40 of D1.

As also pointed out by the examining division, documents D1 (figures 2 and 5, paragraphs [0011] to [0014], [0023]), D6 (figure 3, col. 1, lines 14 to 37, col. 3, lines 1 to 3, col. 4, lines 50 to 60) and D5 (col. 1, lines 4 to 52, col. 4, lines 28 to 46) describe the use of barrier layers to prevent undesired metal diffusion into neighbouring structures. Col. 4, line 61 to col. 5, line 3 of D6 describe that any number or order of layers can be used as long as two metal layers are separated by a diffusion barrier layer. Starting from D1, it would be obvious to include

into the interconnect structure 40 a lowermost and a topmost (or uppermost) diffusion barrier layer in order to solve the objective technical problem. The Board sees no reason to deviate from the examining division's findings concerning the obviousness of feature (A), see section 3.2.3.1 of the Reasons for the Decision. Hence, it appears obvious for the skilled person to modify the interconnect structure known from D1 in view of either D6, or the common general knowledge of the skilled person, or D5 and arrive at a modified interconnect structure having feature (A).

(b) Distinguishing features (B) and (C)

Regarding (B), the partial problem is to improve the adhesion between the interconnect structure in D1 and the substrate 10. As also argued by the examining division, adhesion layers between an interconnect structure and an underlying element (e.g. a semiconductor substrate) are well-known in the technical field of semiconductor devices, see paragraphs [0009] and [0013] of the present application or D2, paragraph [0089]. It is obvious for the skilled person to provide an adhesion layer directly below the modified interconnect structure 40 of D1.

Regarding (C), the Board notes that paragraph [0024] in D1 states that an oxide adhesion layer ([0024], "Oxidschicht als Haftvermittler") can be provided on top of the interconnect structure. When implementing feature (A) to the interconnect structure of D1, the skilled person would provide said oxide adhesion layer directly on the uppermost diffusion barrier layer and hence arrive at a device having feature (C). Anyhow, it would also be obvious for the skilled person to provide an adhesion layer onto the modified interconnect

structure of D1 in order to improve the contact force to e.g. a wire bond.

The appellant did not provide any specific arguments why distinguishing features (B) or (C) would justify an inventive step.

3.2.5 In view of the above considerations, the Board is convinced that the skilled person would arrive at the subject-matter of claim 1 without any inventive skills.

The subject-matter of claim 1 thus lacks an inventive step (Article 56 EPC).

4. First auxiliary request

In its communication pursuant to Article 15(1) RPBA 2020, the Board informed the appellant that it tended to disregard the first auxiliary request pursuant to Article 12(4) RPBA 2007 in conjunction with Article 25(2) RPBA 2020.

Claim 1 according to the first auxiliary request is identical to claim 1 of the second auxiliary request underlying the contested decision, with the exception that feature (j) was added; said second auxiliary request was not admitted into the proceedings by the examining division during the oral proceedings held in the absence of the appellant, see the contested decision, section 4. or the minutes of oral proceedings, last paragraph.

The Board considers that the examining division correctly used their discretion not to admit this second auxiliary request filed one day prior to the oral proceedings, because, in the examining division's

view, it was late-filed, the addition of (e1) did not comply with Article 123(2) EPC and was *prima facie* not suitable to overcome the objection under Article 56 EPC raised against the first auxiliary request underlying the contested decision, because D1 already disclosed feature (e1) in paragraphs [0014] and [0022].

In the statement of grounds of appeal, the appellant merely repeated that feature (e1) might be found in paragraph [0036], without indicating why the examining division was wrong in not admitting the second auxiliary request according to Rule 137(3) EPC or in their judgment that paragraph [0036] did not provide a sufficient basis for feature (e1) or that D1 already disclosed feature (e1).

In any event, the appellant gave no reasons why the semiconductor device structure according to the second auxiliary request underlying the contested decision (or the present first auxiliary request) involved an inventive step over the prior art. It follows that the present auxiliary request does not fulfil the requirements of Article 12(2) RPBA 2007 in combination with Article 25(2) RPBA 2020.

The appellant did not address the admission of the first auxiliary request in its letter dated 26 August 2021.

The Board thus has no reasons to deviate from its provisional opinion and does not admit the first auxiliary request into the proceedings (Article 12(4) RPBA 2007, Article 25(2) RPBA 2020).

5. Second auxiliary request

For claim 1 of the main request the Board already assumed that the first and second adhesion layers are "separate from the interconnect structure". Hence, the subject-matter of claim 1 according to the second auxiliary request lacks an inventive step (Article 56 EPC) for the reasons given for the main request, and is not allowable, irrespective of its admissibility at this stage of the proceedings.

6. As no allowable request is on file, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero S. Ward

Decision electronically authenticated