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Datasheet for the decision of 22 March 2023

Case Number: T 2583/18 - 3.5.04

Application Number: 10852372.1

Publication Number: 2579567

IPC: H04N5/235, H04N5/335

Language of the proceedings: EN

Title of invention:
CMOS IMAGE SENSOR, TIMING CONTROL METHOD AND EXPOSURE METHOD THEREOF

Applicant:
Shenzhen Taishan Online Technology Co., Ltd.

Headword:

Relevant legal provisions:
EPC R. 115(2)
RPBA Art. 12(4), 15(3), 15(5), 15(6)

Keyword:
Late-filed request - request could have been filed in first instance proceedings (yes) - admitted (no)

Decisions cited:
G 0010/93, T 1178/08, T 1212/08, T 1108/10

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 2583/18 - 3.5.04

D E C I S I O N
of Technical Board of Appeal 3.5.04
of 22 March 2023

Appellant: (Applicant)	Shenzhen Taishan Online Technology Co., Ltd. 4/F Fangda Building 12 South Road South Area Hi-Tech Industrial Park Shenzhen Guangdong 518000 (CN)
Representative:	Lapienis, Juozas MSP Europe UAB 21-92 Seimyniskiu Str. 09236 Vilnius (LT)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 7 June 2018 refusing European patent application No. 10852372.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	B. Willems
Members:	M. Paci
	T. Karamanli

Summary of Facts and Submissions

I. The appeal is against the examining division's decision refusing European patent application No. 10 852 372.1, published as international patent application WO 2011/150574 A1.

II. The decision under appeal was based on the grounds that the claims of the main request and the first and second auxiliary requests then on file had not been limited to the invention covered by the supplementary European search report and thus did not meet "*the requirements of Rule 164 EPC in accordance with G 2/92*".

III. The applicant (hereinafter: "appellant") filed notice of appeal. With the statement of grounds of appeal, the appellant filed amended claims 1 to 3 according to a sole request.

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the sole request filed with the statement of grounds of appeal.

IV. On 16 December 2021, a summons to oral proceedings was issued.

V. By letter dated 17 January 2022, the appellant informed the board that "*the Applicant's party is not planning to attend the oral proceedings*".

VI. The board issued a communication under Article 15(1) RPBA 2020 dated 9 January 2023. In this communication, the board gave the following preliminary opinion.

a) The claims of the sole request should have been presented before the department of first instance.

b) The board was inclined to exercise its discretionary power under Article 12(4) RPBA 2007 to hold the sole request inadmissible.

VII. The board held oral proceedings on 22 March 2023.

As announced, the appellant did not attend the oral proceedings.

At the end of the oral proceedings, the Chair announced the board's decision.

VIII. Claim 1 of the appellant's **main request** reads as follows.

"A CMOS image sensor, comprising: a pixel array composed of a plurality of pixel rows, and a control chip for controlling the pixel array; wherein, the pixel array is divided into a plurality of pixel sub-arrays, each pixel sub-array is sequentially controlled by the control chip, and in the control of the pixel sub-array, each of the pixel row of the pixel sub-array is exposed synchronously within an exposure time (T1) under the control of the control chip during one exposure period of the pixel row, and then each pixel row outputs data after waiting for different predetermined waiting times (T2) from the exposure time (T1) under the control of the control chip;

wherein each of the plurality of pixel rows includes the same number of pixel units, each of which includes a photocell (B), a reset transistor (R), a charge overflow gate transistor (T), a row strobe transistor (X) and a source follower (FD), with pixel units in

each pixel column being connected commonly to a first signal outputting transistor (SH1) and a second signal outputting transistor (SH2) of a pixel column containing the pixel unit to output the data; and the control chip sends out, during one exposure period of each pixel row, the following control signals to respectively control the corresponding elements of each pixel unit in the pixel row:

S1: at the beginning of the exposure time (T1), high-level pulses are sent out to turn on the reset transistor (R) and the charge overflow gate transistor (T), respectively;

S2: at the end of the exposure time (T1), a high-level pulse is sent out to turn on the charge overflow gate transistor (T);

S3: at the end of the predetermined waiting time (T2) after the end of the exposure time (T1), high-level pulses are respectively sent out to turn on the row strobe transistor (X) and the first signal outputting transistor (SH1) of the pixel column containing the pixel unit, to sample a signal level;

S4: a high-level pulse is sent out to turn on the reset transistor (R); and

S5: high-level pulses are respectively sent out to turn on the row strobe transistor (X) and the second signal outputting transistor (SH2) of the pixel column containing the pixel unit, to sample a reference level;

wherein the control chip further controls the exposure times (T1) of at least two pixel rows (L1, L2) in the pixel array to be synchronized, the control chip then controls the at least two pixel rows to output the data after respectively waiting for different predetermined waiting times (T2) after the completion of the exposure, and the difference between the predetermined waiting times (T2) of the at least two

pixel rows is not less than the time required for outputting the data by a single pixel row;

wherein the at least two pixel rows (L1, L2) include a first pixel row (L1) with a first predetermined waiting time (T2-1) and a second pixel row (L2) with a second predetermined waiting time (T2-2) and the corresponding control process is as follows:

the control chip simultaneously send [sic] *a high-level pulse to turn on the reset transistors (R) and the charge overflow gate transistors (T) of all pixel units in the first pixel row (L1) and second pixel row (L2), and the exposure will be started after the reset transistors (R) and the charge overflow gate transistors (T) are turned off;*

at the end of the exposure time (T1), the control chip simultaneously sent a high-level pulse to turn on the charge overflow gate transistors (T) of all pixel units in the first pixel row (L1) and second pixel row (L2); charges in the photocells (B) are transferred to the source followers (FD), and then the charge overflow gate transistors (T) are turned off;

the control chip sends, respectively at the end of the first predetermined waiting time (T2-1) and at the end of the second predetermined waiting time (T2-2) after the completion of the exposure time (T1), a control signal to output the data of the first pixel row (L1) and second pixel row (L2); wherein

at the end of the first predetermined waiting time (T2-1) of the first pixel row (L1) after the completion of the exposure time (T1), the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the first pixel row (L1) and to turn on the first signal outputting transistor (SH1) of the pixel column containing the pixel units, to sample the signal level; subsequently, the row strobe transistors (X) of all

pixel units in the first pixel row (L1) and the first signal outputting transistor (SH1) of the pixel column containing the pixel units are turned off, subsequently, the control chip sends out a high-level pulse to turn on the reset transistors (R) of all pixel units in the first pixel row (L1) to empty the charges in the source followers (FD), subsequently, the reset transistors (R) are turned off, subsequently, the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the first pixel row (L1) and to turn on the second signal outputting transistor (SH2) of the pixel column containing the pixel units, to sample the reference level, and the digital signal is obtained from the comparison between the first and second signal outputting transistors (SH1) and (SH2) respectively corresponding to all pixel units in the first pixel row (L1) as the data output of the first pixel row (L1);

wherein at the end of the predetermined waiting time (T2-2) of the second pixel row (L2) after the completion of the exposure time (T1), the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the first pixel row (L1) and to turn on the first signal outputting transistor (SH1) of the pixel column containing the pixel units, to sample the signal level, the row strobe transistors (X) of all pixel units in the second pixel row (L2) and the first signal outputting transistor (SH1) of the pixel column containing the pixel units are turned off, subsequently, the control chip sends out a high-level pulse to turn on the reset transistors (R) of all pixel units in the second pixel row (L2), to empty the charges in the source followers (FD), subsequently, the reset transistors (R) are turned off. Subsequently, the control chip respectively send [sic] *out a high-level*

pulse to turn on the row strobe transistors (X) of all pixel units in the second pixel row (L2) and to turn on the second signal outputting transistor (SH2) of the pixel column containing the pixel units, to sample the reference level, the digital signal is obtained from the comparison between the first and second signal outputting transistors (SH1) and (SH2) respectively corresponding to all pixel units in the second pixel row (L2) as the data output of the second pixel row (L2)."

Reasons for the Decision

1. The appeal is admissible.

Non-attendance of the appellant at the oral proceedings before the board

2. The duly summoned appellant did not attend the oral proceedings. However, under Rule 115(2) EPC, the proceedings could continue without that party. In accordance with Article 15(3) RPBA 2020, which is applicable in accordance with Article 25(1) RPBA 2020, the board relied on the appellant's written submissions for its decision. The board was in a position to announce a decision at the conclusion of the oral proceedings since the case was ready for decision (Article 15(5) and (6) RPBA 2020, which applies in accordance with Article 25(1) RPBA 2020) and the appellant's voluntary absence was not a reason for delaying the decision (Article 15(3) RPBA 2020).

Sole request - admittance under Article 12(4) RPBA 2007

3. In the case in hand, the statement of grounds of appeal was filed before the date on which the revised version of the Rules of Procedure of the Boards of Appeal (RPBA 2020) entered into force, i.e. 1 January 2020 (see OJ EPO 2019, A63). Thus, in accordance with Article 25(2) RPBA 2020, Article 12(4) to (6) RPBA 2020 does not apply to the question of whether to admit the sole request. Instead, Article 12(4) of the RPBA in the 2007 version (RPBA 2007 - see OJ EPO 2007, 536) continues to apply.

4. Under Article 12(4) RPBA 2007, the board has the discretionary power to hold inadmissible facts, evidence or requests which could have been presented or were not admitted in the first-instance proceedings. Since, in fact, almost every claim request could have been presented before the department of first instance, the question within that context is whether the situation was such that the filing of this request should already have taken place at that stage (see Case Law of the Boards of Appeal of the European Patent Office, 10th edition 2022, "Case Law", V.A.5.11.1 and V.A.5.11.4(a)). The board exercises its discretion under Article 12(4) RPBA 2007 having regard to the particular circumstances of the individual case (see e. g. decision T 1178/08, point 2.3 of the Reasons). However, as was held in G 10/93 (OJ EPO 1995, 172, point 4 of the Reasons), "*[p]roceedings before the boards of appeal in ex-parte cases are primarily concerned with examining the contested decision*". Appeal proceedings are not a continuation of examination at first instance or a second, parallel procedure for the substantive examination otherwise to be carried out by the examining division which

applicants could freely opt to launch depending on the circumstances (see Case Law, V.A.5.11.4(a), in particular the cited decisions T 1108/10 and T 1212/08).

5. According to the appellant, the claims of the sole request are "*based on the claims submitted on 22.05.2014, which claims have been searched and examined by the Examining Division*" (see statement of grounds of appeal, page 1). The board construes this statement to mean that the appellant was asserting that the claims of the current sole request were based on claims 1 to 7 of the sole request filed by letter of 22 May 2014.

6. However, the board notes that the claims of the current sole request differ extensively from the claims of the sole request filed by letter of 22 May 2014 as follows:

(a) Claims 1, 2 and 3 have been combined into new claim 1.
(b) Claims 3, 4 and 5 have been combined into new claim 3.
(c) Claims 8 to 13 have been deleted.
(d) The following features, which were **not** in any of claims 1 to 7 of 22 May 2014, have been introduced into claims 1 and 3:

"wherein the at least two pixel rows (L1, L2) include a first pixel row (L1) with a first predetermined waiting time (T2-1) and a second pixel row (L2) with a second predetermined waiting time (T2-2) and the corresponding control process is as follows:
the control chip simultaneously send [sic] *a high-level pulse to turn on the reset transistors (R) and the charge overflow gate transistors (T) of all pixel units*

in the first pixel row (L1) and second pixel row (L2), and the exposure will be started after the reset transistors (R) and the charge overflow gate transistors (T) are turned off;
at the end of the exposure time (T1), the control chip simultaneously sent a high-level pulse to turn on the charge overflow gate transistors (T) of all pixel units in the first pixel row (L1) and second pixel row (L2); charges in the photocells (B) are transferred to the source followers (FD), and then the charge overflow gate transistors (T) are turned off;
the control chip sends, respectively at the end of the first predetermined waiting time (T2-1) and at the end of the second predetermined waiting time (T2-2) after the completion of the exposure time (T1), a control signal to output the data of the first pixel row (L1) and second pixel row (L2); wherein
at the end of the first predetermined waiting time (T2-1) of the first pixel row (L1) after the completion of the exposure time (T1), the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the first pixel row (L1) and to turn on the first signal outputting transistor (SH1) of the pixel column containing the pixel units, to sample the signal level; subsequently, the row strobe transistors (X) of all pixel units in the first pixel row (L1) and the first signal outputting transistor (SH1) of the pixel column containing the pixel units are turned off, subsequently, the control chip sends out a high-level pulse to turn on the reset transistors (R) of all pixel units in the first pixel row (L1) to empty the charges in the source followers (FD), subsequently, the reset transistors (R) are turned off, subsequently, the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel

units in the first pixel row (L1) and to turn on the second signal outputting transistor (SH2) of the pixel column containing the pixel units, to sample the reference level, and the digital signal is obtained from the comparison between the first and second signal outputting transistors (SH1) and (SH2) respectively corresponding to all pixel units in the first pixel row (L1) as the data output of the first pixel row (L1); wherein at the end of the predetermined waiting time (T2-2) of the second pixel row (L2) after the completion of the exposure time (T1), the control chip respectively sends out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the first pixel row (L1) and to turn on the first signal outputting transistor (SH1) of the pixel column containing the pixel units, to sample the signal level, the row strobe transistors (X) of all pixel units in the second pixel row (L2) and the first signal outputting transistor (SH1) of the pixel column containing the pixel units are turned off, subsequently, the control chip sends out a high-level pulse to turn on the reset transistors (R) of all pixel units in the second pixel row (L2), to empty the charges in the source followers (FD), subsequently, the reset transistors (R) are turned off. Subsequently, the control chip respectively send [sic] *out a high-level pulse to turn on the row strobe transistors (X) of all pixel units in the second pixel row (L2) and to turn on the second signal outputting transistor (SH2) of the pixel column containing the pixel units, to sample the reference level, the digital signal is obtained from the comparison between the first and second signal outputting transistors (SH1) and (SH2) respectively corresponding to all pixel units in the second pixel row (L2) as the data output of the second pixel row (L2)."*

7. According to the appellant, the above additional features were taken from paragraphs [0079] to [0085] of the description of the application as filed (see statement of grounds of appeal, page 3).

8. During the proceedings before the examining division, the applicant had several opportunities to file the claims of the current sole request, namely in response to the communication pursuant to Article 94(3) EPC dated 11 December 2015, in response to the communication pursuant to Article 94(3) EPC dated 15 September 2017 and during the oral proceedings, which the applicant chose not to attend.

9. If the board were to admit the current sole request into the appeal proceedings, it would have to examine and decide on the extensively amended claims of this request for the first time on appeal (see additional features under point 6(d) above), or remit the case to the department of first instance for further prosecution. Neither procedural option is appropriate. These two inappropriate options would never have arisen if the amended claims in question had been presented in the proceedings before the examining division. The appellant should have allowed the examining division to exhaustively assess and then decide on all subject-matter for which the appellant intended to seek protection, even if only on a subsidiary basis, if it wished the board to decide on it. This approach is also in line with established case law (see Case Law, V.A. 5.11.4(a)).

10. For the above reasons, the board exercises its discretionary power under Article 12(4) RPBA 2007 to hold the appellant's sole request inadmissible.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Boelicke B. Willems

Decision electronically authenticated