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Datasheet for the decision of 19 June 2023

Case Number: T 0890/19 - 3.5.06

Application Number: 05732778.5

Publication Number: 1745344

IPC: G06F1/32

Language of the proceedings: EN

Title of invention:
A MOBILE APPARATUS COMPRISING INTEGRATED CIRCUIT AND METHOD OF POWERING DOWN SUCH CIRCUIT

Applicant:
SnapTrack, Inc.

Headword:
Sequential logic/SNAPTRACK

Relevant legal provisions:
EPC 1973 Art. 84

Keyword:
Claims - clarity (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
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Beschwerdekammern

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Case Number: T 0890/19 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 19 June 2023

Appellant: (Applicant)	SnapTrack, Inc. 5775 Morehouse Drive San Diego, CA 92121 (US)
Representative:	Wagner & Geyer Partnerschaft mbB Patent- und Rechtsanwälte Gewürzmühlstrasse 5 80538 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 October 2018 refusing European patent application No. 05732778.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	M. Müller
Members:	G. Zucka
	B. Müller

Summary of Facts and Submissions

I. The appeal is against the decision by the examining division, dispatched with reasons on 25 October 2018, to refuse European patent application 05732778.5, on the basis that the subject-matter of the independent claims 1 and 8 was not inventive, Article 56 EPC 1973.

II. A notice of appeal was received on 3 January 2019, the appeal fee being paid on the same day. A statement of grounds of appeal was received on 26 February 2019.

III. The appellant requested that the decision under appeal be set aside and a patent granted on the basis of the claims that were the subject of the refusal. The appellant made a conditional request for oral proceedings.

IV. The board issued a summons to oral proceedings. In an annex to the summons, the board set out its preliminary opinion on the appeal.

V. On 19 May 2023, the appellant filed claims of an auxiliary request.

VI. The appellant requests that the decision under appeal be set aside and a European patent be granted on the basis of the claims of the main request filed with a letter of 22 August 2018 or the auxiliary request filed with a letter of 19 May 2023.

VII. Independent claim 1 of the main request reads as follows:

"A mobile apparatus comprising an integrated circuit to operate predefined functions, the circuit being susceptible to be set in a standby operating mode from which said circuit can resume operation within a predefined period of time, said circuit comprising sequential logic having defined states, the mobile apparatus further comprising a power down unit for storing relevant states of the sequential logic into a state recovery storage area during standby mode;

said circuit comprising different logic blocks to distinguish between configuration sequential logic and functional sequential logic, so that only the states of the configuration sequential logic are relevant to be stored into said state recovery storage area."

VIII. Independent claim 1 of the auxiliary request reads as follows:

"A mobile apparatus comprising an integrated circuit to operate predefined functions, the circuit being susceptible to be set in a standby operating mode from which said circuit can resume operation within a predefined period of time, wherein said circuit is an Input/Output peripheral circuit to enable said mobile apparatus to communicate with peripheral devices, said circuit comprising sequential logic having defined states, the mobile apparatus further comprising a power down unit for storing relevant states of the sequential logic into a state recovery storage area during standby mode;

wherein said sequential logic comprises configuration sequential logic and functional sequential logic,

wherein configuration sequential logic consists of configuration state machines and state registers including flip-flops and contains all the necessary

information for the function of the Input/Output peripheral block, determining operation, settings and behavior of the Input/Output peripheral block, wherein, after reset, the configuration sequential logic has a well-defined state;

wherein functional sequential logic also consists of flip-flops, but its state is not relevant when the Input/Output peripheral block is not used, wherein the functional sequential logic performs functions of synchronization, internal data RAM operations, state machines, FIFOs and shift registers, wherein the content of functional sequential logic does not have to be saved before power down;

said circuit comprising different logic blocks to distinguish between configuration sequential logic and functional sequential logic, so that only the states of the configuration sequential logic are stored into said state recovery storage area."

IX. At the end of the oral proceedings, the chairman announced the board's decision.

Reasons for the Decision

1. *The invention*

The application relates to mobile apparatuses comprising an IC which can be placed in a standby mode (description, page 1, lines 2-4).

The aim of the application is to reduce the standby current by minimising the leakage current (*ibid.*, page 1, lines 22-23).

To achieve this, the IC comprises sequential logic having defined states, relevant states of the sequential logic being stored into a state recovery storage area during standby mode (*ibid.*, page 1, lines 26-28). This allows minimisation of the powered logic, resulting in a reduction of the leakage current (*ibid.*, page 2, lines 1-2).

2. *Clarity, Article 84 EPC 1973*

2.1 *Main request*

2.1.1 As regards claim 1 of the main request, the terms "configuration sequential logic" and "functional sequential logic" are non-standard terms.

2.1.2 At the end of claim 1, the wording "so that only the states of the configuration sequential logic are relevant to be stored into said state recovery storage area" does not imply any concrete limitation on the claimed apparatus, which might shed light on the meaning of the terms in question. It merely refers to the relevance of certain states for potential storage ("to be stored"), but the actual storage of the states in the state recovery storage area is not clearly part of the claim's definition.

2.1.3 The appellant effectively argues (see response to the summons, page 1, last paragraph, with reference to T 169/20, items 1 through 1.3.4, the Guidelines for Examination IV-F, 4.2, and T 190/99) that if a claim contains a hitherto unused term, that term does not necessarily need to be defined in the claim but the claim may rely on a definition given in the

description. In the case in hand, specific reference was made to page 5, lines 3 to 26 of the description.

Whether or to what extent this is indeed allowable does not need to be decided in the present case, given that the description does not contain a clear definition of "configuration sequential logic" and "functional sequential logic" either (see the following section).

2.2 *Auxiliary request*

2.2.1 The explanations on "configuration sequential logic" and "functional sequential logic", given in the description on page 5, lines 6 to 13, have been introduced in claim 1 of the auxiliary request. The further text referred to by the appellant (page 5, lines 14-26) does not contain any further details defining the terms in question, nor has the appellant argued that this was so. This means that claim 1 of the auxiliary request defines the terms in question in the best possible way within the limits of the contents of the application as originally filed.

2.2.2 The term "configuration sequential logic" is defined in such manner that it "consists of configuration state machines and state registers including flip-flops and contains all the necessary information for the function of the Input/Output peripheral block, determining operation, settings and behavior of the Input/Output peripheral block, wherein, after reset, the configuration sequential logic has a well-defined state"

In this definition, it remains unclear which information is "necessary" for the function of the Input/Output peripheral block. In the board's understanding this depends on parameters and circumstances undefined in

the claims, especially which "predefined functions" are provided and what it takes to "resume operation", or what "within a predefined period of time" means, and on choices made by the skilled person in function of their wishes or preferences, both of which may vary over time.

2.2.3 The term "functional sequential logic" is defined in such manner that it "also consists of flip-flops, but its state is not relevant when the Input/Output peripheral block is not used, wherein the functional sequential logic performs functions of synchronization, internal data RAM operations, state machines, FIFOs and shift registers, wherein the content of functional sequential logic does not have to be saved before power down".

Also here, it is not clear what it means for a state to be "relevant". Again, in the board's understanding this depends on undefined parameters and circumstances and on subjective and variable user preferences.

2.3 *Conclusion*

As a consequence, claim 1 of the auxiliary request does not satisfy the requirements of Article 84 EPC 1973. Moreover, claim 1 of the main request lacks clarity, either due to the use of undefined and non-standard terminology in the claim or, as discussed in view of the auxiliary request, because the explanations given in the description for the terms are unclear in themselves.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

L. Stridde Martin Müller

Decision electronically authenticated