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Datasheet for the decision of 31 January 2022

Case Number: T 0983/19 - 3.5.05

Application Number: 15192930.4

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Language of the proceedings: EN

Title of invention:
CONTROL SYSTEM AND METHOD FOR CACHE COHERENCY

Applicant:
VIA Alliance Semiconductor Co., Ltd.

Headword:
CONTROL SYSTEM FOR CACHE COHERENCY / VIA

Relevant legal provisions:
EPC Art. 56
RPBA 2020 Art. 13(1), 13(2)

Keyword:
Inventive step - (no) - effect not made credible within the whole scope of claim

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Case Number: T 0983/19 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 31 January 2022

Appellant: (Applicant)	VIA Alliance Semiconductor Co., Ltd. Room 301 No. 2537, Jinke Road Zhangjiang Hi-Tech Park Shanghai 201203 (CN)
Representative:	Michalski Hüttermann & Partner Patentanwälte mbB Speditionstraße 21 40221 Düsseldorf (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 17 October 2018 refusing European patent application No. 15192930.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	N. H. Uhlmann
	D. Prietzel-Funk

Summary of Facts and Submissions

I. The appellant appealed against the examining division's decision refusing the European patent application in suit.

II. The examining division decided that the claims of the main request did not meet the requirements of Article 123(2) EPC. Furthermore, it decided that the claims of the auxiliary requests 1 and 2 did not satisfy the requirements of Articles 56 and 84 EPC.

III. The examining division made reference *inter alia* to the following documents:

D1 US 2013/311725
D2 EP 2 570 920.

IV. With the statement setting out the grounds of appeal, the appellant maintained the main request and submitted amended auxiliary requests 1 and 2.

V. The board summoned the appellant to oral proceedings.

In a communication under Article 15(1) RPBA 2020, the board set out its provisional opinion on the case.

VI. With a letter dated 10 January 2022, the appellant submitted a sole request replacing all previous requests on file.

VII. The appellant's final requests were that the decision under appeal be set aside and that a patent be granted based on the sole, main request submitted with the letter dated 10 January 2022.

VIII. Claim 1 of the sole request reads as follows:

"A control method for cache coherency, comprising:

providing a first electrical device (110) and a second electrical device (130), the first electrical device (110) having a first operating system and the second electrical device (130) having a second operating system, wherein the first electrical device (110) and the second electrical device (130) are different devices (110, 130), and wherein the first device (110) is a subscriber device and the second device (130) is a host device;

coupling the first electrical device (110) to the second electrical device (130) by a cache coherency, CC, interface (120), the CC interface (120) being a bus-interface external to the first electrical device (110) and the second electrical device (130);

transmitting, by a first processing unit (111) of the first electrical device (110), a link-connect request to the second electrical device (130) when the first electrical device (110) is coupled to the second electrical device (130) by the cache coherency CC interface (120);

establishing, by the CC interface (120), a link between the first electrical device (110) and second electrical device (130) according to the link connect request;

pre-storing, by the second electrical device (130), status information of the second operating system of the second electrical device (130), before the first operating system of the first electrical device (110) is operated by the second processing unit (131) of the second electrical device (130)

performing, by the second electrical device (130), a re-initiate operation for a plurality of hardware elements of the second electrical device (130) to make the first operating system obtain related information of the plurality of hardware elements of the second

electrical device (130) after the status information of the second operating system of the second electrical device (130) has been stored;

after the re-initiate operation, performing, by the first operating system, an enumeration operation to the plurality of hardware elements of the second electrical device (130) to obtain the related information of the hardware elements of the second electrical device to make the first operating system be able to be operated in the second electrical device (130), after obtaining the related information of the hardware elements of the second electronic device (130);

operating, by the second processing unit (131) of the second electrical device (130), the first operating system of the first electrical device (110); and

maintaining, by the CC interface (120), data coherency between the first electrical device (110) and second electrical device (130), when the first operating system of the first electrical device (110) is operated by the second processing unit (131) of the second electrical device (130)."

Reasons for the Decision

1. The application in suit pertains to a method and system for executing an operating system from one computing device on another, connected computing device. It is claimed that a cache coherency interface is used to establish a link between the devices.

2. Document D2 discloses techniques for executing applications and operating systems designed for one computing platform on another computing platform.

3. Admission

The sole request on file addresses, and resolves, clarity and added-matter objections, some of which were raised for the first time in the board's preliminary opinion under Article 15(1) RPBA 2020. Consequently, the board decided to admit it under Article 13(1) and (2) RPBA 2020.

4. The claims meet the requirements of Articles 84 and 123(2) EPC.

5. Inventive step

5.1 Document D2 forms a suitable starting point for the following inventive-step analysis.

5.2 The subject-matter of claim 1 is distinguished from the disclosure of D2 by the following features:

(a) the link is provided by a cache coherency interface;

(b) performing, by the first operating system, an enumeration operation to the plurality of hardware elements of the second electrical device to obtain the related information of the hardware elements of the second electrical device; and

(c) maintaining, by the CC interface, data coherency between the first electrical device and second electrical device, when the first operating system of the first electrical device is operated by the second processing unit of the second electrical device.

5.3 The appellant did not argue that feature (a) contributed towards an inventive step. The board likewise does not see any inventive contribution.

5.4 The features (a), (b) and (c) do not lead to any combined technical effect.

5.5 With regard to feature (b), the board holds that it is suggested in document D2. In particular, the source device 10 (corresponding to the first device as claimed) comprises a platform control manager 70 (Figure 2, paragraph 20). The manager performs a negotiation between the source device 10 and target device 100 and a determination of the compatibility of versions of the source OS with the target device platform (paragraph 20, claim 8). This implies that information of the hardware elements of the second electrical device is obtained. Consequently, D2 discloses "to obtain the related information of the hardware elements of the second electrical device". It is apparent that, depending on the target hardware platform, different versions of the source OS will be sent to, and executed on, the target device.

The appellant argued that the teaching in D2 that OS compatibility is determined (paragraph 20) is not the same as the allegedly claimed "adapting the OS". This argument is not convincing. Claim 1 does not require that the OS must be adapted but only that it is to be made able to be operated on the second device. Furthermore, the selection of a version of the OS that is directed to the target device in D2 makes the OS able to be operated on the second device.

Performing an enumeration operation is a commonly used technique. The application in suit does not ascribe any specific advantage to the enumerating. Likewise, the appellant did not submit any arguments specifically pertaining to the enumeration operation.

5.6 The appellant argued that the normal meaning of the term "data coherency" as used in feature (c) was "that

all memories are continuously updated such that all memories have the same content".

It may be that, normally, memories are continuously updated. However,

- claim 1 pertains not to the normal use but to a very special use of cache coherency;
- claim 1 does not refer to any memories;
- according to the application in suit, the first processor may go to sleep (current dependent claim 3; description page 9, lines 17 to 21, page 10, lines 18 and 19). Furthermore, upon disconnection and resumption of processing on the first device, data is synchronised (page 10, lines 1 to 6). This would be unnecessary if continuous updates had taken place.

Hence, feature (c) cannot be understood in such a specific and narrow sense.

5.7 The appellant argued that feature (c) led to the effects "keeps the electrical device, the operating system of which is run on the other device, up to date" and "when the operation of the operating system of this device on the other device is stopped and the operation of this device is resumed, this device is operable right away".

Such effects are not achieved over the claimed scope. In particular, the application in suit teaches that data synchronisation may be needed (see above in section 5.6), i.e. the first device would not be operable right away.

5.8 Document D1 discloses two processing circuitries 10 and 50. They are different devices because they have different micro-architectures and different numbers of

cores (Figure 1 and paragraph 87). The interconnect 70 according to D1 corresponds to the claimed bus interface and is external to the two processing circuitries (Figure 1).

5.9 D1 discloses data coherency as claimed during the snooping period 240 to 245 in Figure 3; see also the last sentence in paragraphs 108 and 92.

5.10 The appellant argued that the skilled person would not consider document D1 because D1 did not disclose different operating systems.

However, claim 1 does not require that the operating systems be different.

5.11 The appellant submitted that D1 did not disclose that all memories are continuously and bi-directionally updated such that all memories have the same content.

This argument is not convincing. Claim 1 cannot be interpreted to include such features (see section 5.6 above). For example, when the first processor goes into sleep mode (page 10, lines 18 and 19, claim 3), then no bi-directional update takes place.

5.12 The appellant argued that the synchronisation mentioned on page 10, line 3 of the description of the application in suit referred to operating system data only and not to application data. The latter was updated continuously via cache coherency.

The board disagrees. The description and the claims of the application in suit do not distinguish between operating system data and application data. Additionally, lines 5 and 6 on page 10 refer to "the data that has been processed by the second electrical device". This wording clearly encompasses any data processed by the second device.

5.13 For these reasons, none of the distinguishing features (a), (b) and (c) contributes towards inventive step. Hence, the subject-matter of claim 1 does not involve an inventive step (Article 56 EPC).

6. Consequently, the sole request on file is not allowable. With no allowable request on file the appeal is not allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

A. Chavinier Tomsic A. Ritzka

Decision electronically authenticated